

THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION, INVENTEC CORPORATION, 2017 ALL RIGHT RESERVED.

NOTES:
1.HSF Property;Comply iSupplier system HSF property attribute up-to-date value.

THRONE

15KBL MD U22 & R U42

SVT BUILD

2017.08.09

18-Apr-2017		
DATE	CHANGE NO.	REV

DESIGN / DRAWER	XXX	DATE	18-Apr-2017
CHECK	BRYAN CHIOU		
APPROVAL	TICKY TSAI		
FILE NAME	R10_TOPAZ_WS		
PCB PIN	6050A2940901	PCB VER	A01

INVENTEC			
TITLE			
Throne R15			
SIZE	COLL	DOC NUMBER	REV
A3	G	1310xxxxx-0-0	X01
SHEET		of 24	

Index

1 COVER
2 INDEX
3 BLOCK DIAGRAM
4 POWER PROCEDURE
5 CHARGER
6 P3V3A_P5V0A
7 P5V0_SYS
8 DDR POWER
9 P2V5
10 P1V8A
11 P1V0A
12 VCORE & GT & GA
13 VCORE
14 VCCGT
15 VCCSA
16 BOM MAP U22/R42
17 AMP 12V
18 LCM POWER
19 ENABLE PIN
20 SYSTEM POWER
21 PCB SCREW
22 DDR4-1
23 DDR4-2
24 DDR4-3
25 DDR4-4

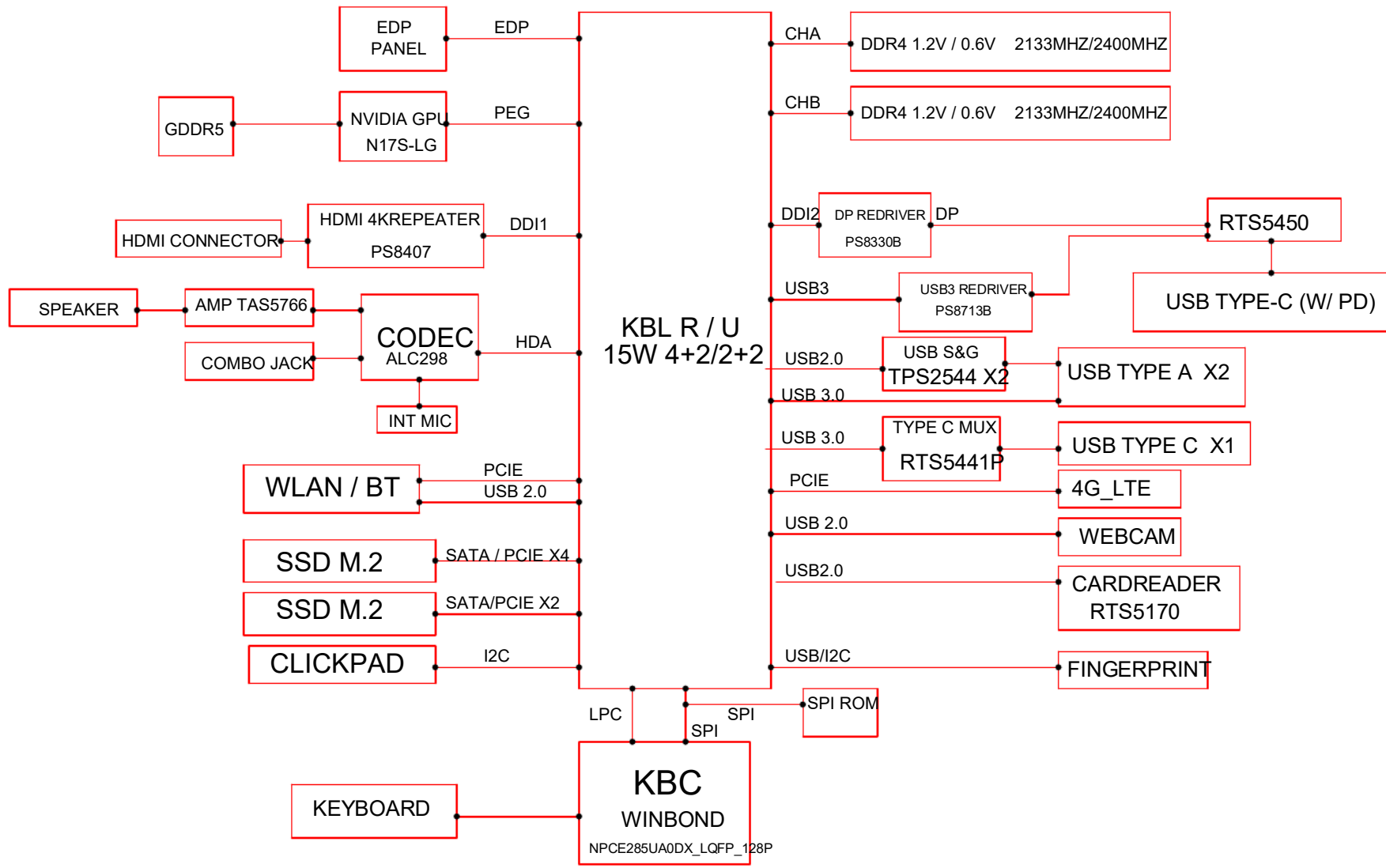
26 CPU-DDR
27 CPU-LPC, SPI, SMBUS, CLINK
28 CPU-GPIO
29 CPU-MISC, HDA, SDIO, JTAG
30 CPU-PCIE, USB3, USB2
31 CPU-CLK, RTC, CFG
32 CPU-DDI, EDP, CSI2, EMMC
33 CPU-POWER MANAGEMENT
34 CPU-POWER1
35 CPU-POWER2
36 CPU-POWER3
37 CPU-GND, CFG, RSVD
38 EC_NPCE285
39 KB_CONN & LED
40 TOUCH CONN/LID SWITCH
41 CODEC ALC298
42 AUDIO JACK
43 AMP TI5766
44 CARDREADER RTS5170
45 USB3.0 CONN1
46 USB3.0 CONN2
47 USB3 REDRIVER
48 TYPE C RTS5441P
49 TYPE C CONN1
50 WLAN ON BOARD
51 4G_LTE
52 NGFF_M.2 SSD1

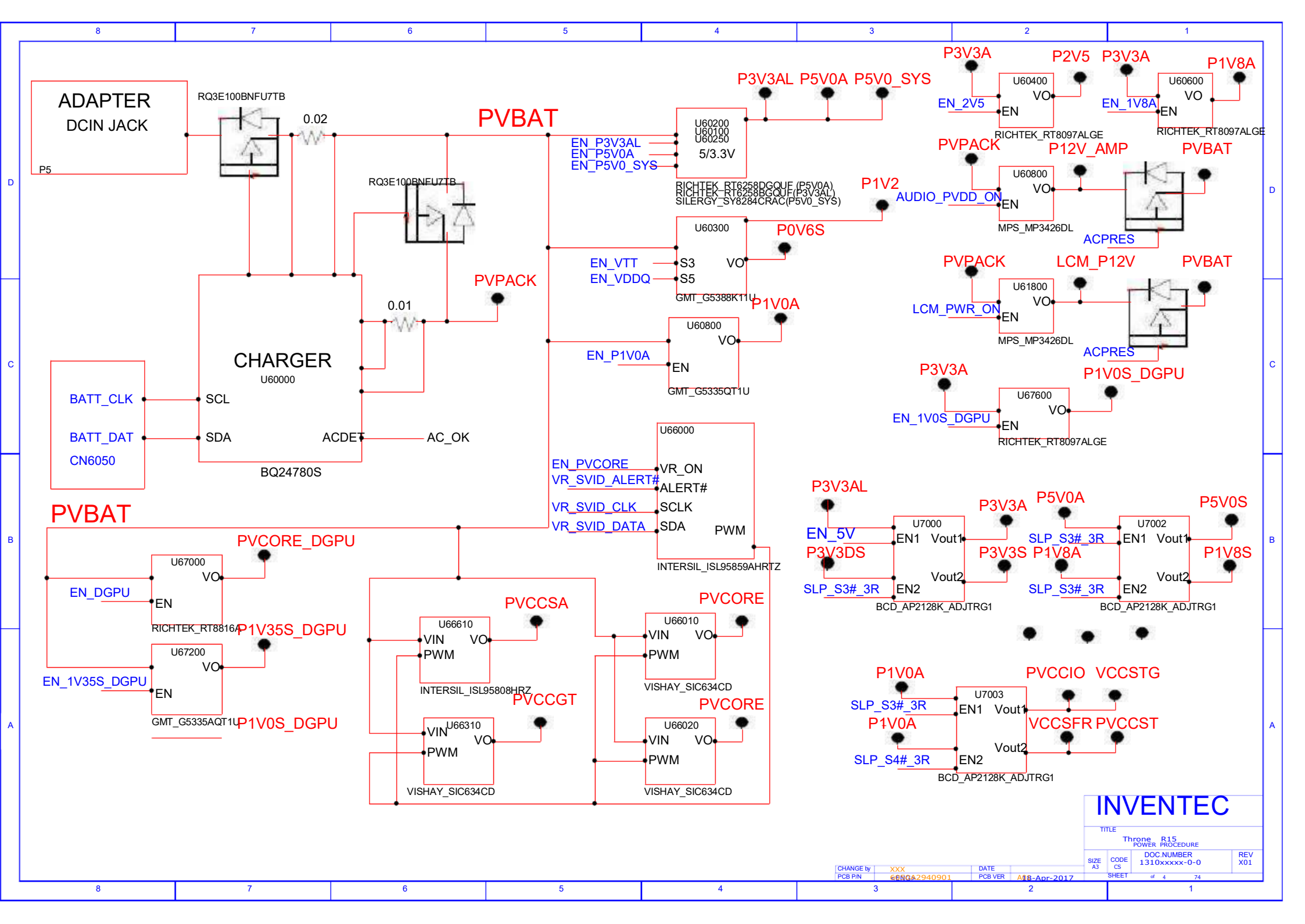
53 NGFF M.2 SSD2
54 DP REDRIVER
55 USB3 REDRIVER
56 TYPE C RTS5450
57 TYPE C CONN2
58 EDP CN
59 CAMERA
60 FAN
61 HDMI 4K\2K
62 HDMI CONN
63 GPU COVER
64 GPU-1
65 GPU-2
66 GPU-3
67 GPU-4
68 GPU-5
69 GDDR5 VRAM
70 DGPU_RT8816A
71 DGPU_P1V35
72 DGPU_P1V0S
73 GPU POWER SEQUENCE
74 EMI

INVENTEC

TITLE Throne R15 INDEX			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET of 2 74			

CHANGE by PCB PIN	XXX 6650A2940901	DATE PCB VER	A08-Apr-2017
----------------------	---------------------	-----------------	--------------





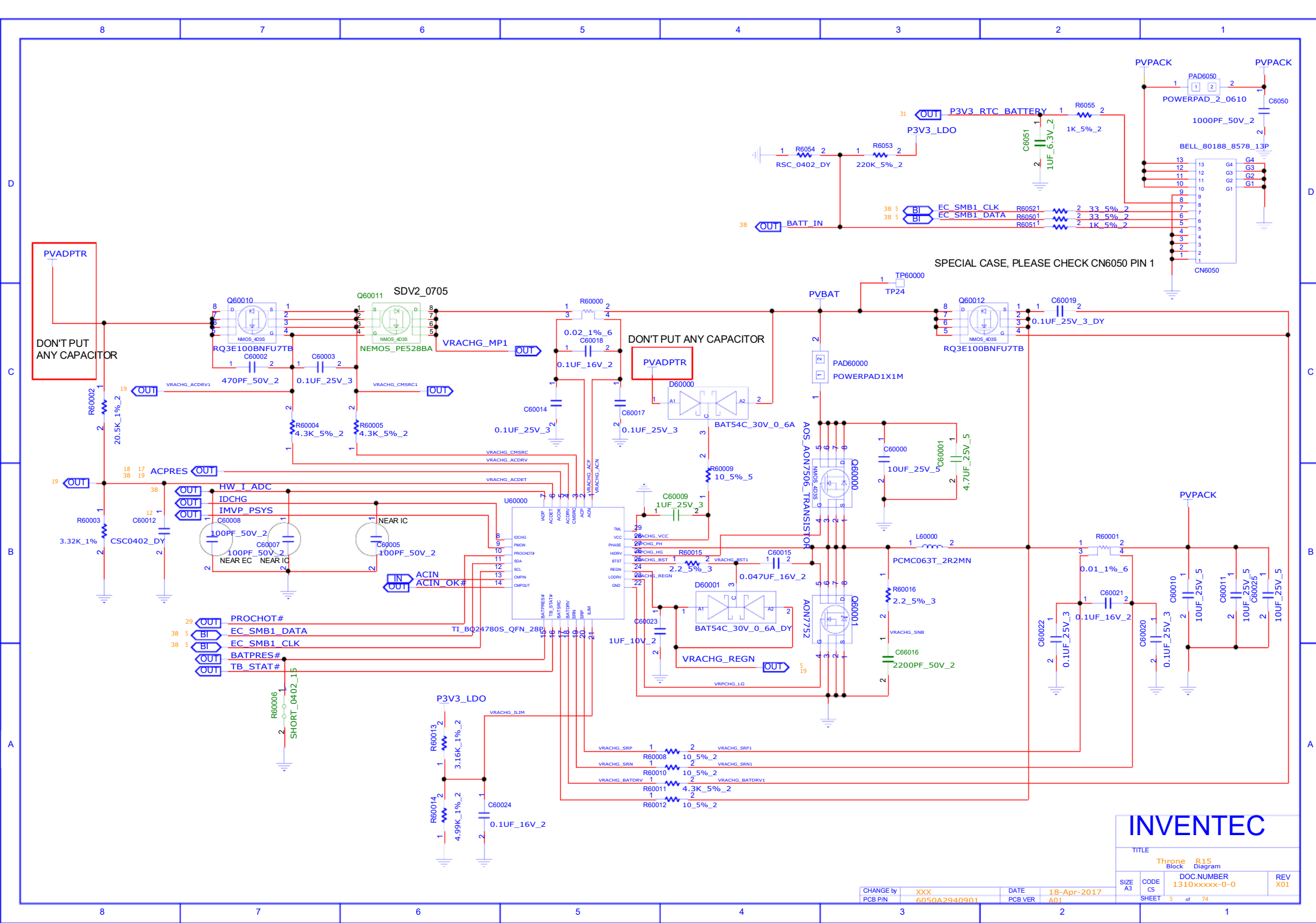
INVENTEC

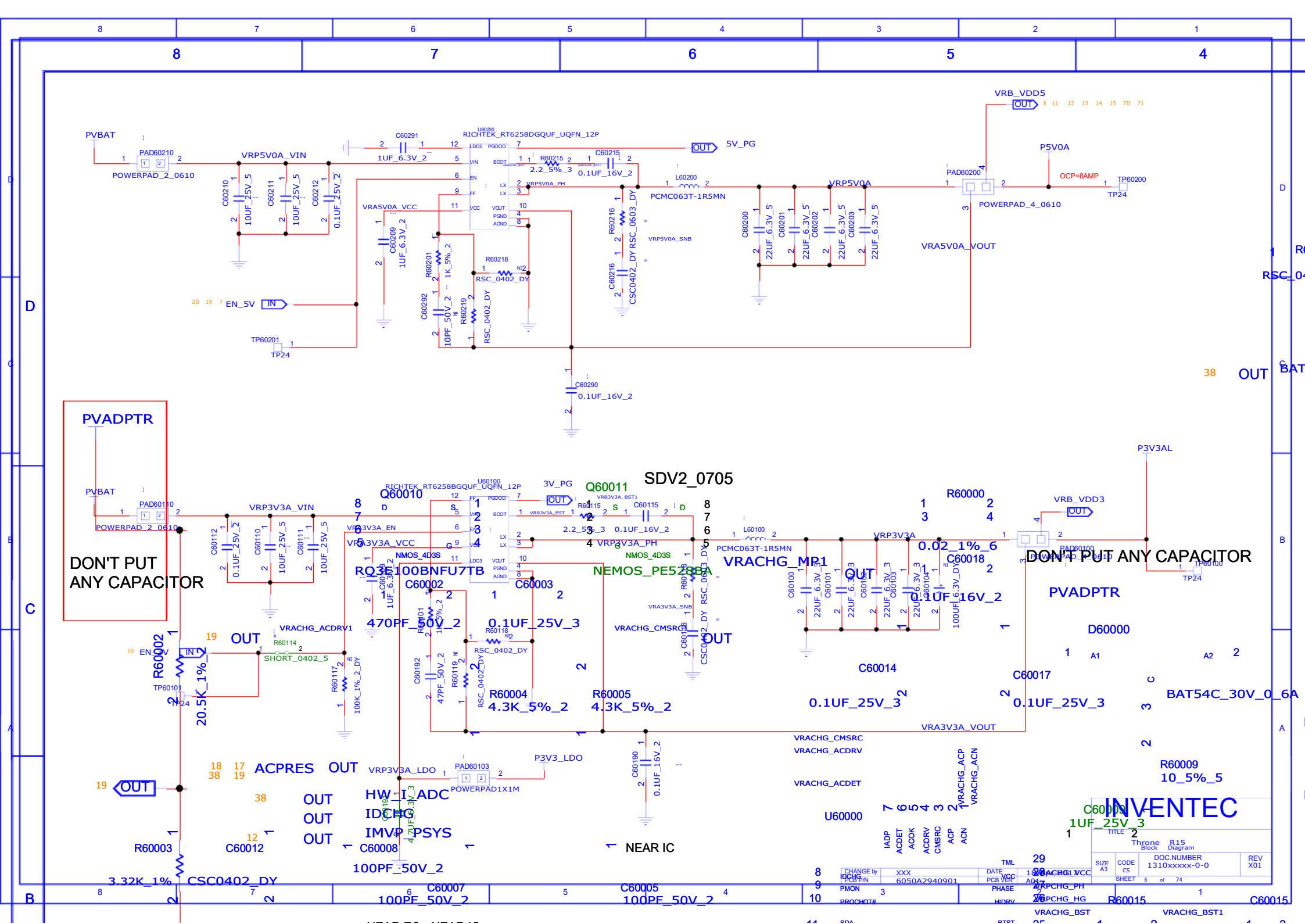
TITLE
Throne R15
POWER PROCEDURE

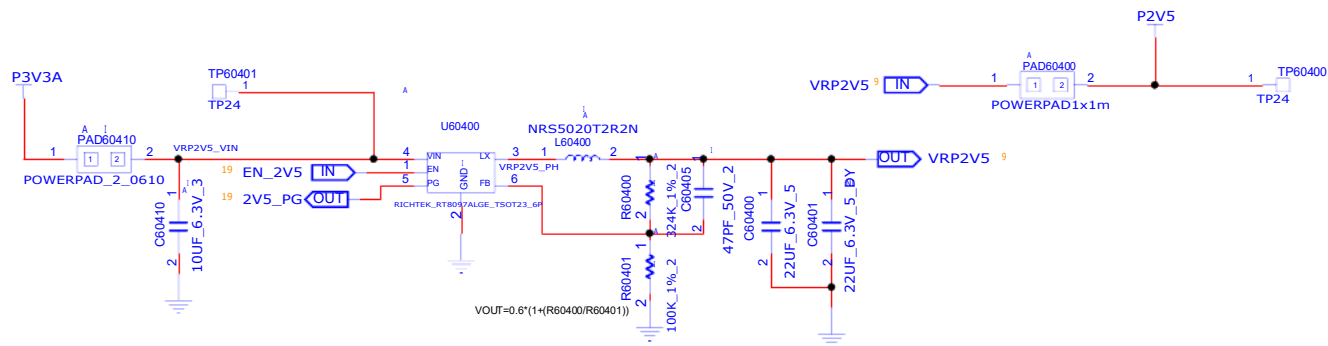
SIZE CODE DOC NUMBER
A3 CS 1310xxxx-0-0

SHEET of 4 74
REV X01

CHANGE by XXX
PCB P/N GRGA2940901
DATE PCB VER A18-Apr-2017







INVENTEC

TITLE
Throne R15
Block Diagram

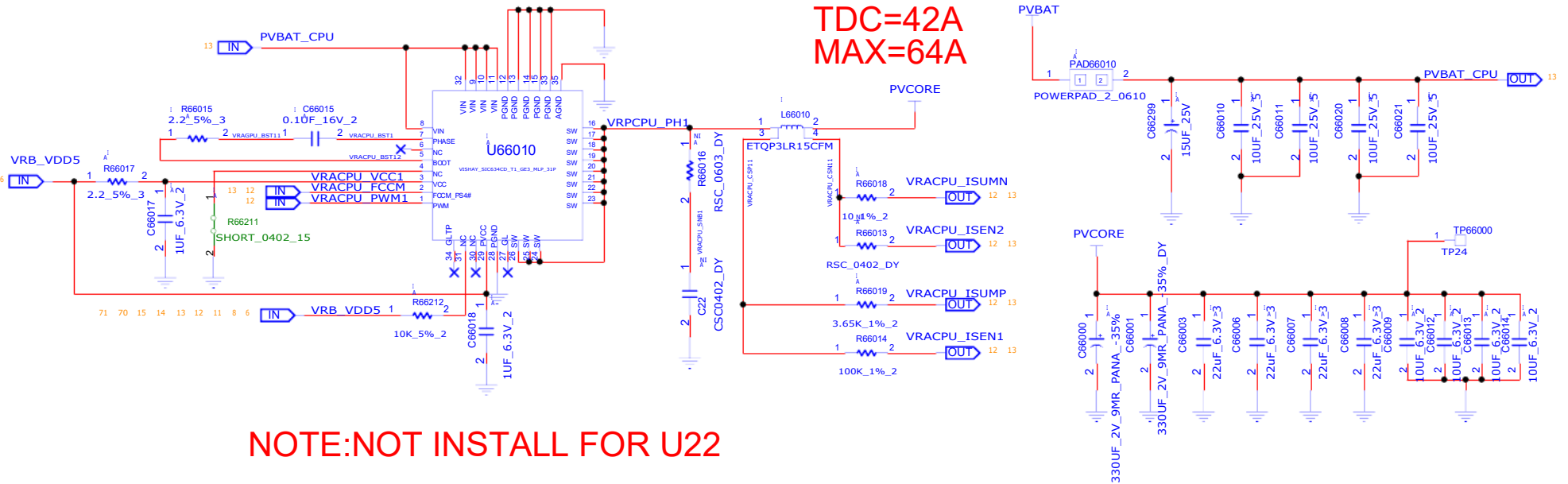
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 9	of 74		

CHANGE by PCB P/N	XXX 6050A2940901	DATE PCB VER	18-Apr-2017 A01
----------------------	---------------------	-----------------	--------------------

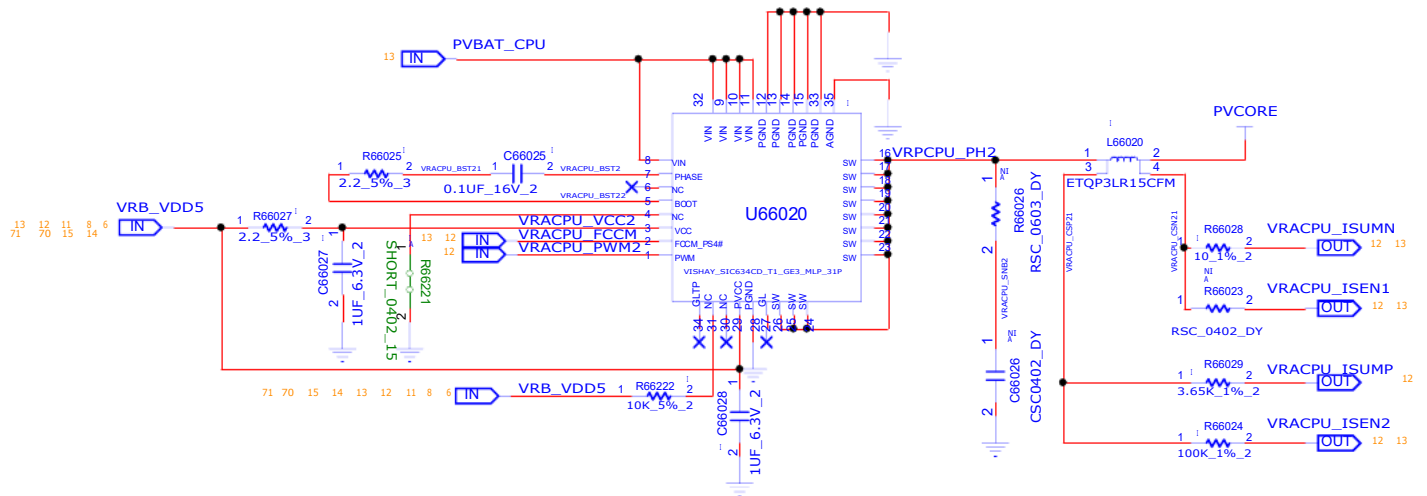
CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

NOTE:ONE PHASE FOR U22

TDC=42A
MAX=64A



NOTE:NOT INSTALL FOR U22

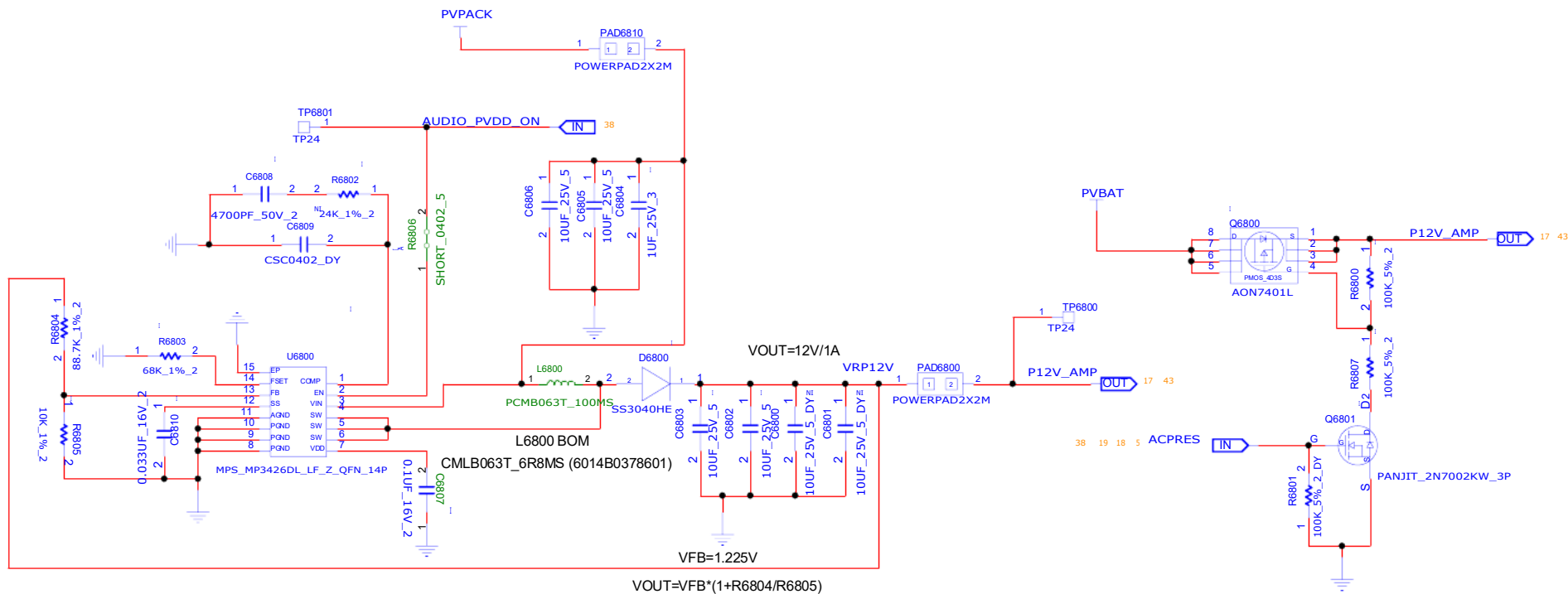


INVENTEC

TITLE			
Throne R15 Diagram			
DOC NUMBER 1310xxxxx-0-0			
SIZE A3	CODE CS	SHEET 13 of 74	REV X01

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

U42			U22		
Location	IEC P/N	Description	Location	IEC P/N	Description
C88150	6010B0046101	CAP-CHIP,0.047UF,16V,K,X7R,0402,TAP	C88150	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP
C88151	6010B0010101	CHIP,0.033UF,16V,K,X7R,0402,TR	C88151	6010B0010101_DY	CHIP,0.033UF,16V,K,X7R,0402,TR
R88006	60130B0000ZT_DY	RES-CHIP-0OHM-5%-1/16W-0402-TAP	R88006	60130B0000ZT	RES-CHIP-0OHM-5%-1/16W-0402-TAP
R88007	60130B0000ZT_DY	RES-CHIP-0OHM-5%-1/16W-0402-TAP	R88007	60130B0000ZT	RES-CHIP-0OHM-5%-1/16W-0402-TAP
C88155	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP	C88155	6010A0000101_DY	CAP-CHIP-223-K,16V-X7R-0402-TAP
C88156	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP	C88156	6010A0000101_DY	CAP-CHIP-223-K,16V-X7R-0402-TAP
R88154	6013A008780S	RES-CHIP-383-1%-1/16W-0402-TAP	R88154	6013A008780D	RES-CHIP-287-1%-1/16W-0402-TAP
R88171	6013A0088207	RES-CHIP-3.65K-1%-1/16-0402-TAP	R88171	6013B00097601	RES-CHIP,1.69K,1%,1/16W,0402,TAP
R88107	6013A0088708	RES-CHIP-107K-1%-1/16-0402-TAP	R88107	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP
C88020	6010B0150801	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM	C88020	6010B0150801_DY	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM
C88021	6010B0150801	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM	C88021	6010B0150801_DY	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM
R88014	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP	R88014	6013A0014701_DY	RES-CHIP-100K-1%-1/16W-0402-TAP
U88020	6019B1530201	IC,MOSFET DRIVER,40A,MLP55-31L,31P,TR	U88020	6019B1530201_DY	IC,MOSFET DRIVER,40A,MLP55-31L,31P,TR
L88020	6014B0341701	INDUCTOR,0.15UH,+/- 20%,1MHZ,29A,7.3X8.7X3MM,SMD,TR	L88020	6014B0341701_DY	INDUCTOR,0.15UH,+/- 20%,1MHZ,29A,7.3X8.7X3MM,SMD,TR
R88025	60130B2R200T	RES-CHIP-2.2-5%-1/10W-0803-TAP	R88025	60130B2R200T_DY	RES-CHIP-2.2-5%-1/10W-0803-TAP
C88025	6010A0036403	CHIP,0.1UF,16V,K,X7R,0402,TAP	C88025	6010A0036403_DY	CHIP,0.1UF,16V,K,X7R,0402,TAP
R88027	60130B2R200T	RES-CHIP-2.2-5%-1/10W-0803-TAP	R88027	60130B2R200T_DY	RES-CHIP-2.2-5%-1/10W-0803-TAP
C88027	6010B0392101	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR	C88027	6010B0392101_DY	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR
C88028	6010B0392101	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR	C88028	6010B0392101_DY	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR
R88024	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP	R88024	6013A0014701_DY	RES-CHIP-100K-1%-1/16W-0402-TAP
R88028	6013A0014201	RES-CHIP-10OHM-1%-1/16W-0402-TAP	R88028	6013A0014201_DY	RES-CHIP-10OHM-1%-1/16W-0402-TAP
R88029	6013A0088207	RES-CHIP-3.65K-1%-1/16-0402-TAP	R88029	6013A0088207_DY	RES-CHIP-3.65K-1%-1/16-0402-TAP
R88222	60130B1030ZT	CHIP,10K,5%,1/16W,0402,TR	R88222	60130B1030ZT_DY	CHIP,10K,5%,1/16W,0402,TR
C88000	6010B0136301	CAPACITOR-AL-SP,330UF,2V,-35%/+10%,105C,DX1.9,SMD,TR,9MOHM	C88000	6010B0219101	SP,220UF,2V,M,105C,DX1.9,SMD,TR,6MOHM

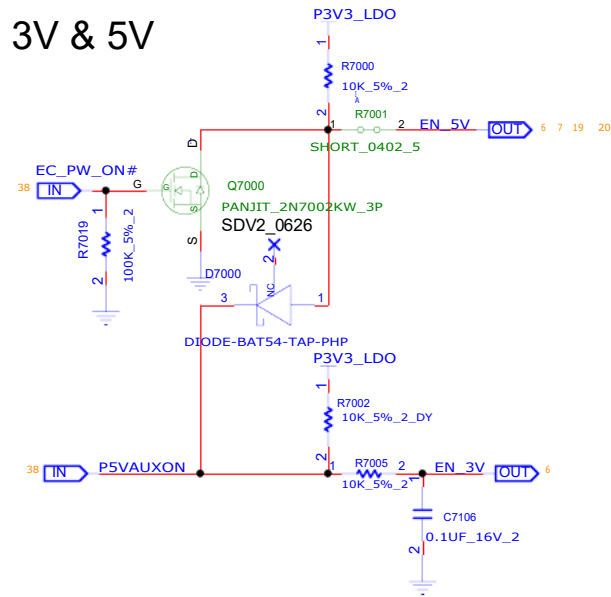


INVENTEC

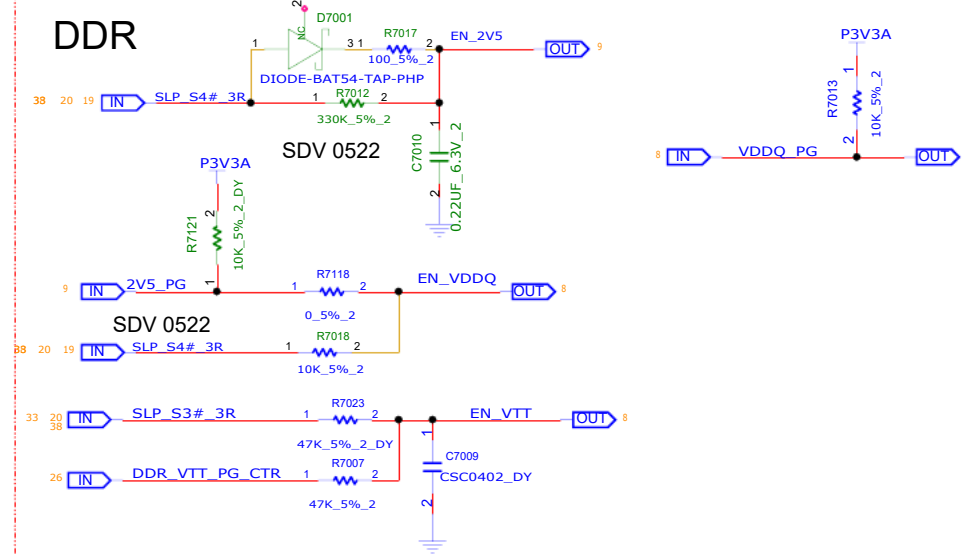
TITLE			
Throne R15 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 17	of 74		

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

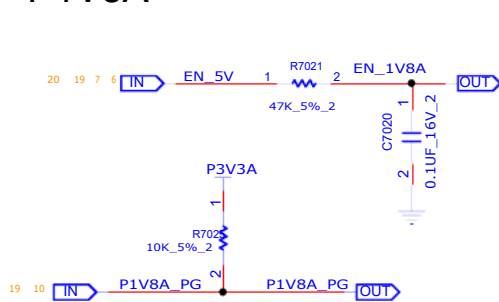
3V & 5V



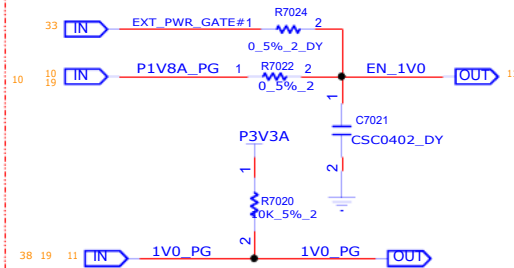
DDR



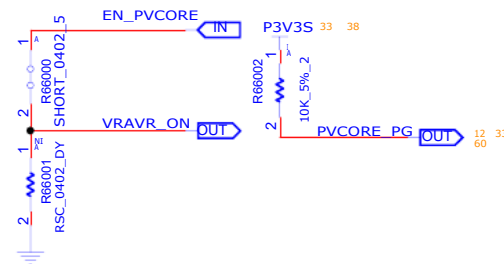
P1V8A



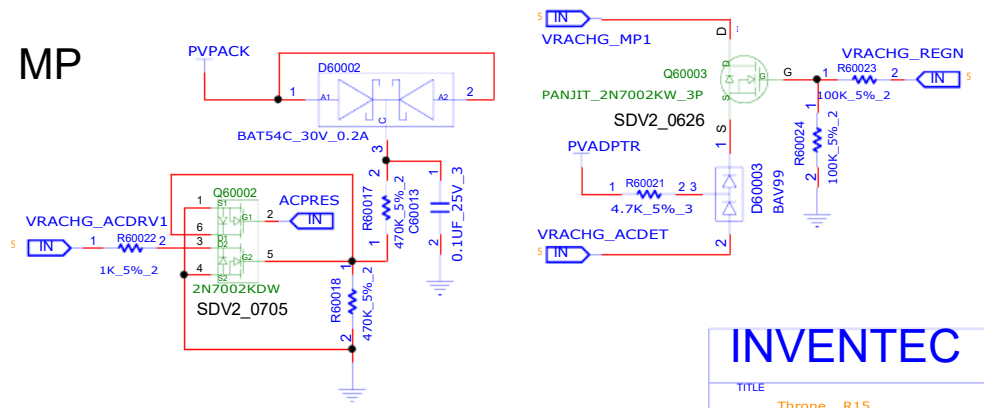
P1V0A



PVCORE

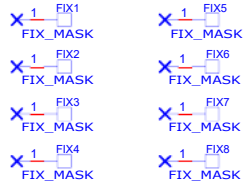
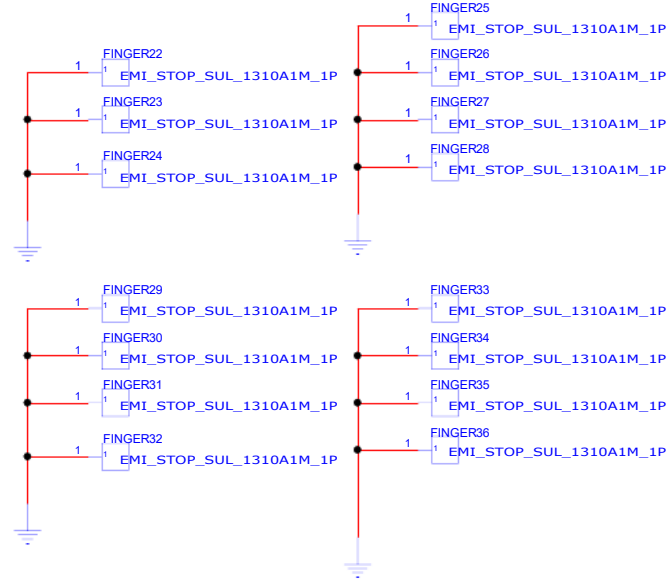
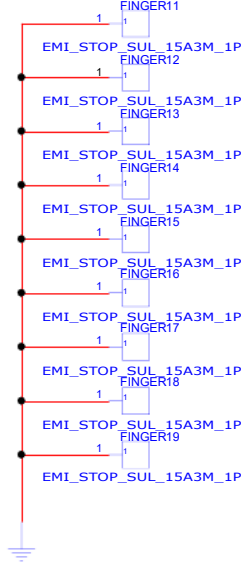
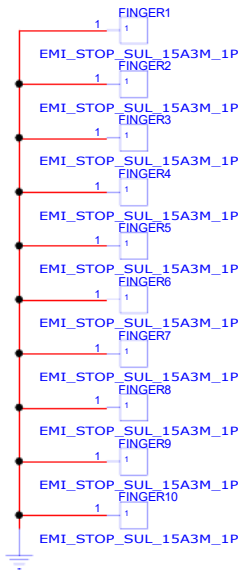


MP

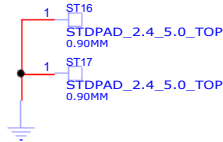


INVENTEC

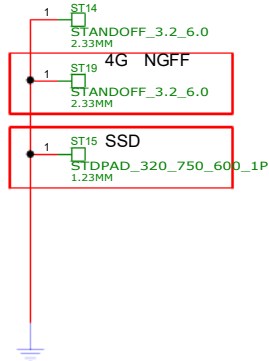
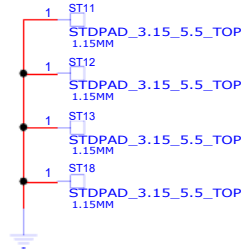
REFERENCE 0~49(PCB SCREW)



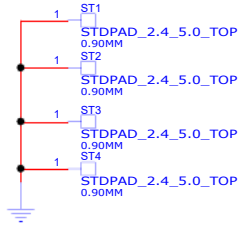
GPU



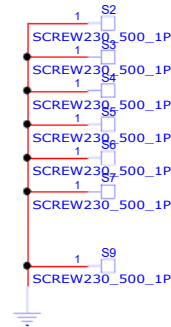
FAN



CPU



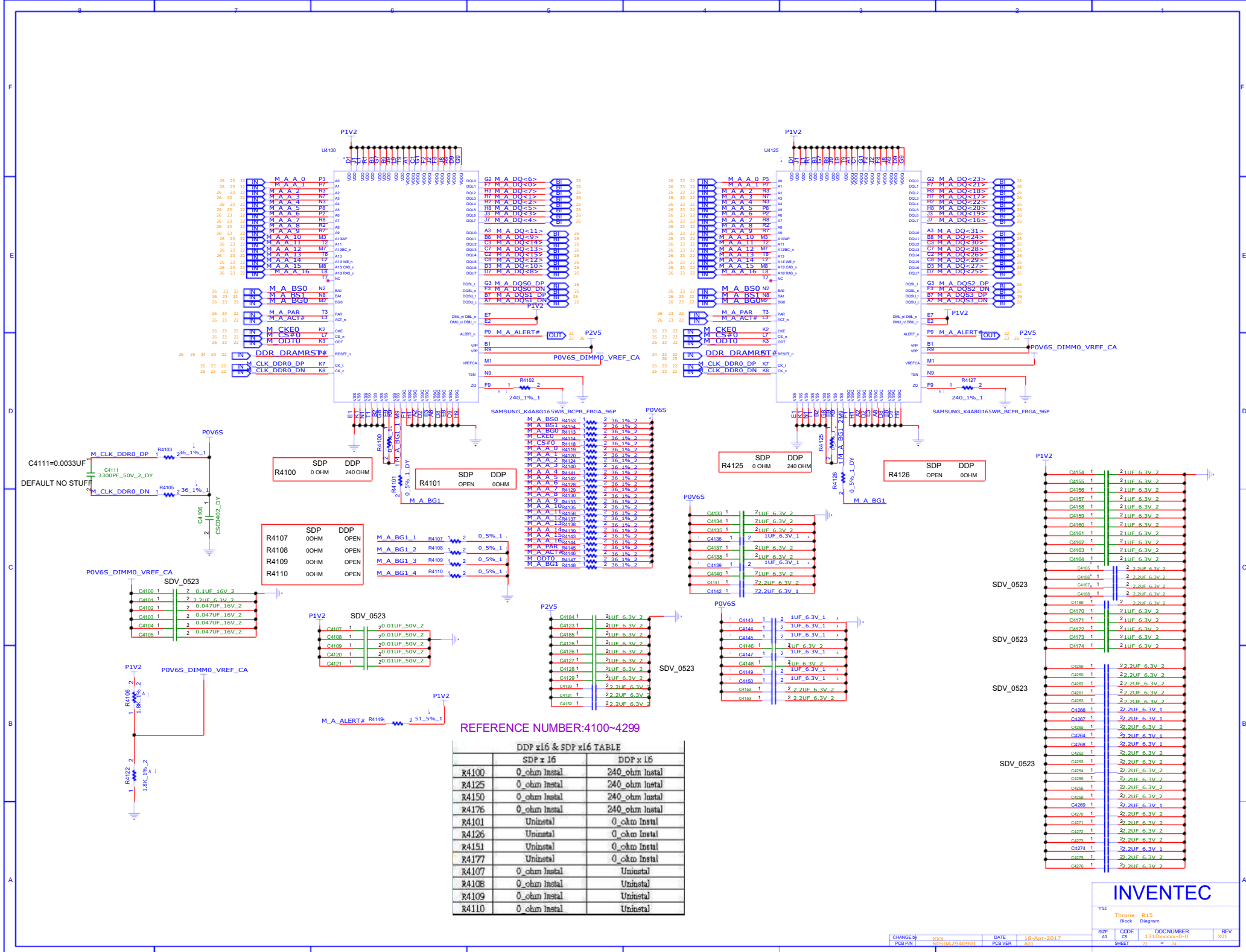
PCB

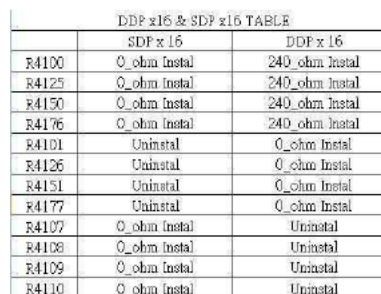


INVENTEC

TITLE			
Throne R15 Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		21 of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

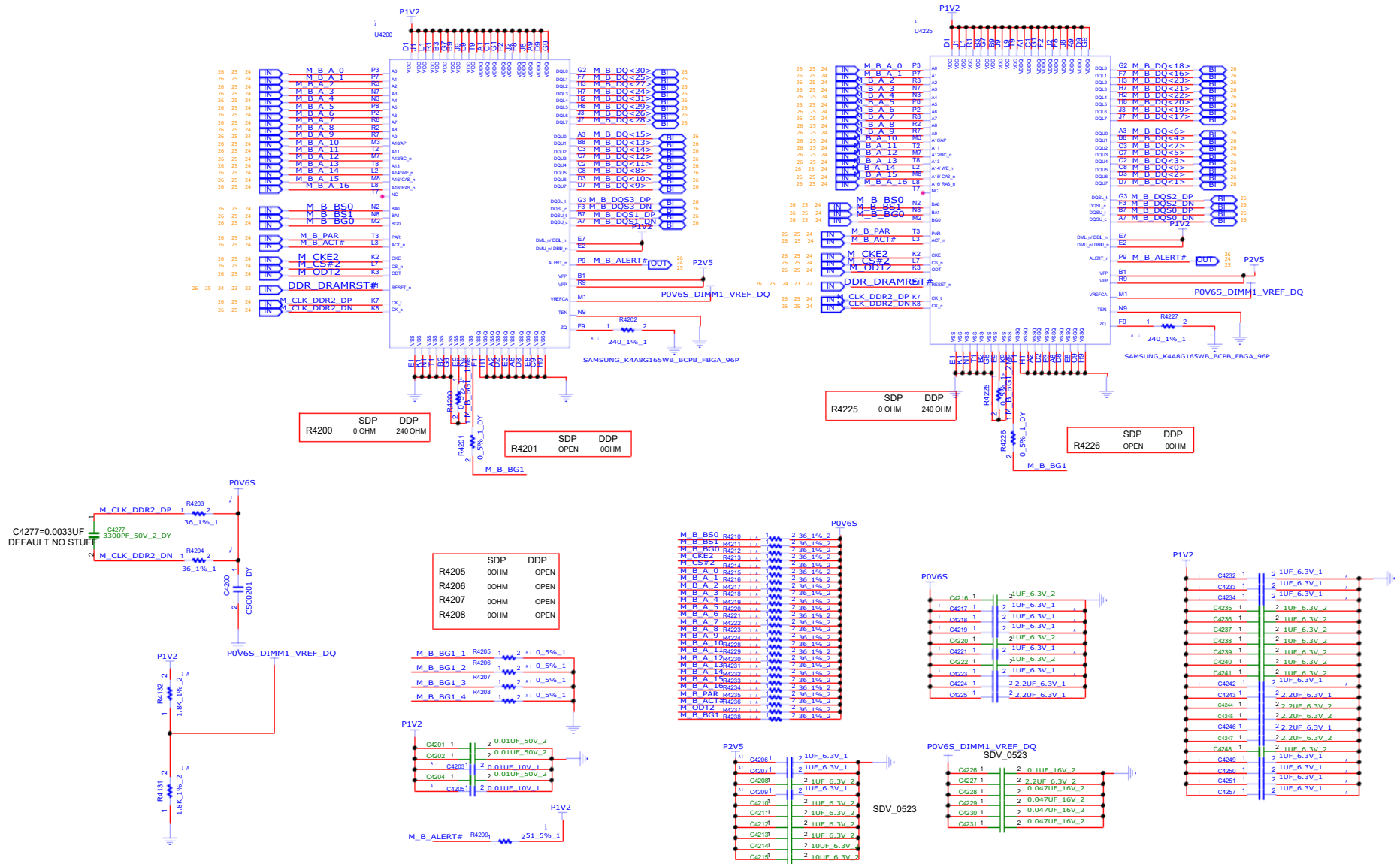




TITLE			
Throne		R15	
Block		Diagram	
SIZE A3	CODE CS	DOCNUMBER 1310xxxxx-0-0	REV X01
SHEET		23	of 74

F
E
D
C
B
A

F
E
D
C
B
A

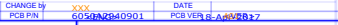


REFERENCE NUMBER:4100~4299

INVENTEC

Title		Throne R15
Block Diagram		
SIZE	A3	CODE
PCB PIN	XXXX	DOCNUMBER
DATE	18-Apr-2017	REV
PCB VER	A01	X01
SHEET	20	of 20

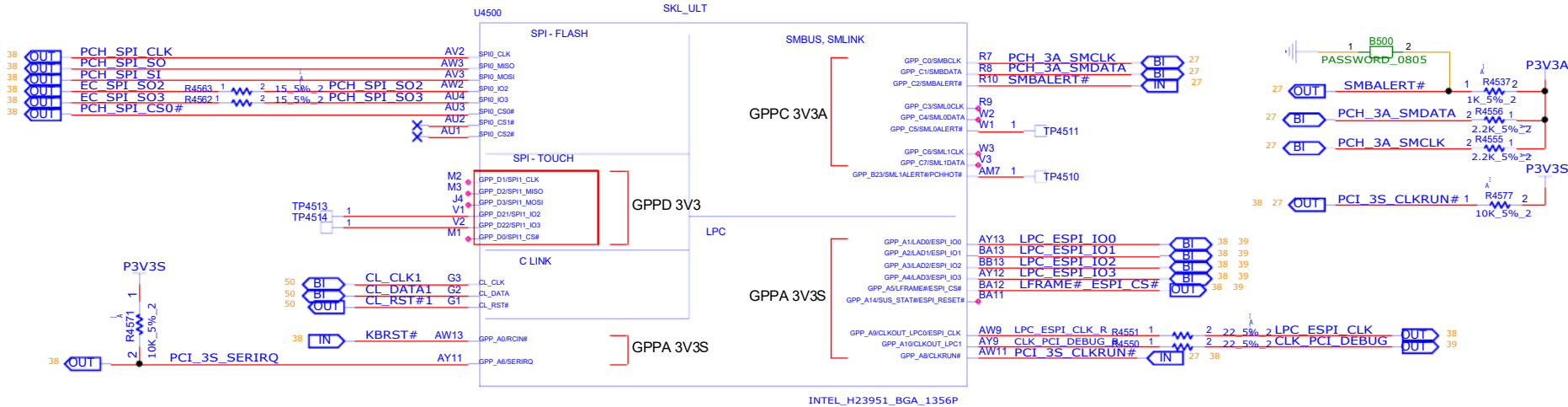
CHANGE BY XXX G050A2940901 DATE 18-Apr-2017 PCB VER A01



543016 60.3.31: ALL UNUSED GPIOs (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION
All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The
Internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPD9W_3p3	3.3V



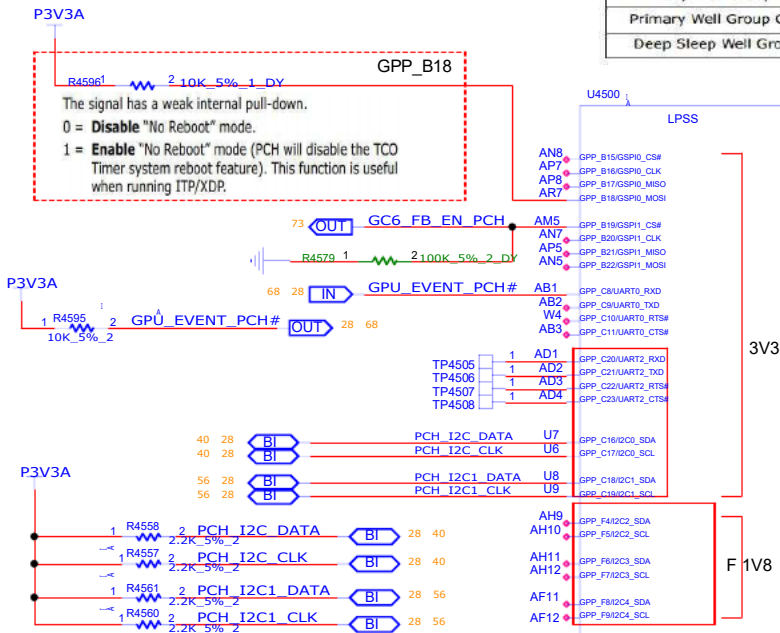
REFERENCE 4700~4949(PCH)

543016 60.3.31: ALL UNUSED GPIOs (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

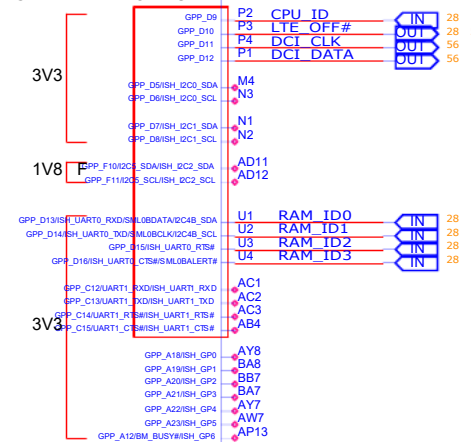
GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



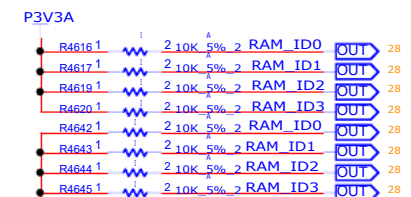
INTEL_H23951_BGA_1356P

INTEGRATED SENSOR HUB



RAM ID

	RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID
DIMM	0	0	0	0
SAMSUNG 4G	0	0	0	1
SAMSUNG 8G	0	0	1	0
K6A6G165MB-M3CIC K6A6G165MB-M3CIC	0	0	1	0
SAMSUNG 16G	0	0	1	1
K6A6G165MB-M3CIC K6A6G165MB-M3CIC	0	0	1	1
HYNIX 4G	0	1	0	0
HYNIX 8G	0	1	0	1
H5AN8GB64R1UHC H5AN8GB64R1UHC	0	1	0	1
HYNIX 16G	0	1	1	0
H5AN8GB64R1UHC H5AN8GB64R1UHC	0	1	1	0
MICRO 4G	0	1	1	1
MICRO 8G	1	0	0	0
MICRO 16G	1	0	0	1



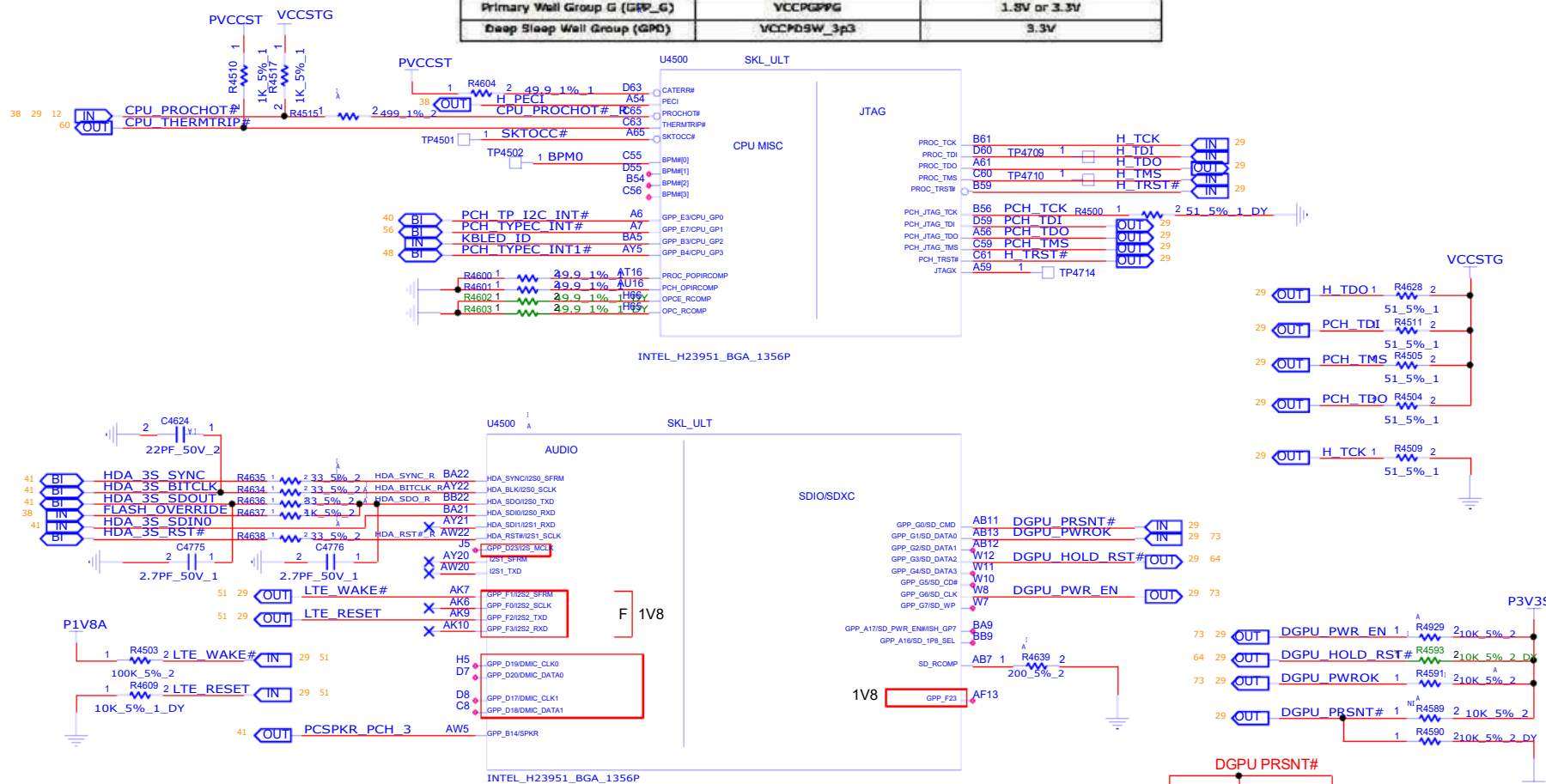
INVENTEC

TITLE			
Throne R15 Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01

CHANGE by	XENG>	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A1VER>

All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



The signal has a weak internal pull-down. **GPP_B14**
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) or cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handed through FITC).

DGPU PRSNT#	
DIS	0
UMA	1

INVENTEC

TITLE			
Throne Block R15 Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 29 of 74			

Table 24-3. PCI Express® Link Configurations Supported

SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port9		Port11	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port5		Port7					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9			

Notes:
1. A PCIe Lane is composed of a single pair of Rx and Tx signals (such as, Rx3+/Rx3- and Tx3+/Tx3- make up PCIe Lane 3). A PCIe Link is composed of one or more PCIe Lanes (such as bundling 2 PCIe Lanes together would make a x2 PCIe Link). A PCIe Link is addressed by the lowest number PCIe Port it connects to in the PCH (such as a x2 PCIe Link connected to PCIe Ports 3 and 4 would be called x2 PCIe Port 3).

Figure 12-4. PCIe_RCOMP and PCIe_RCOMPN Connections

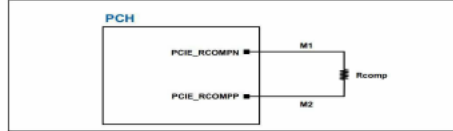
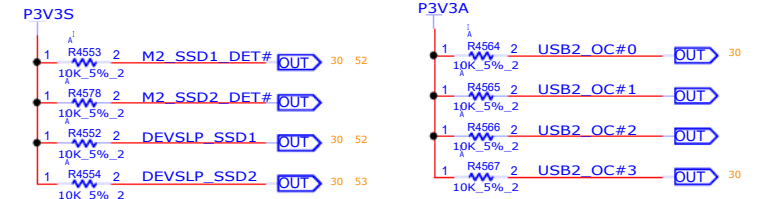


Table 12-9. PCI Express® Compensation Routing Guidelines

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length	Length Matching
PCIe_RCOMP	M1: 4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.3 ohms).	At least 1.2 mils to any adjacent high speed I/O.	100 ohm +/-1% external resistor between RCOMP and RCOMPN	NA	Both RCOMP & RCOMPN need to be matched to less than 1% trace and board
PCIe_RCOMPN	M2: 4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.3 ohms).			NA	



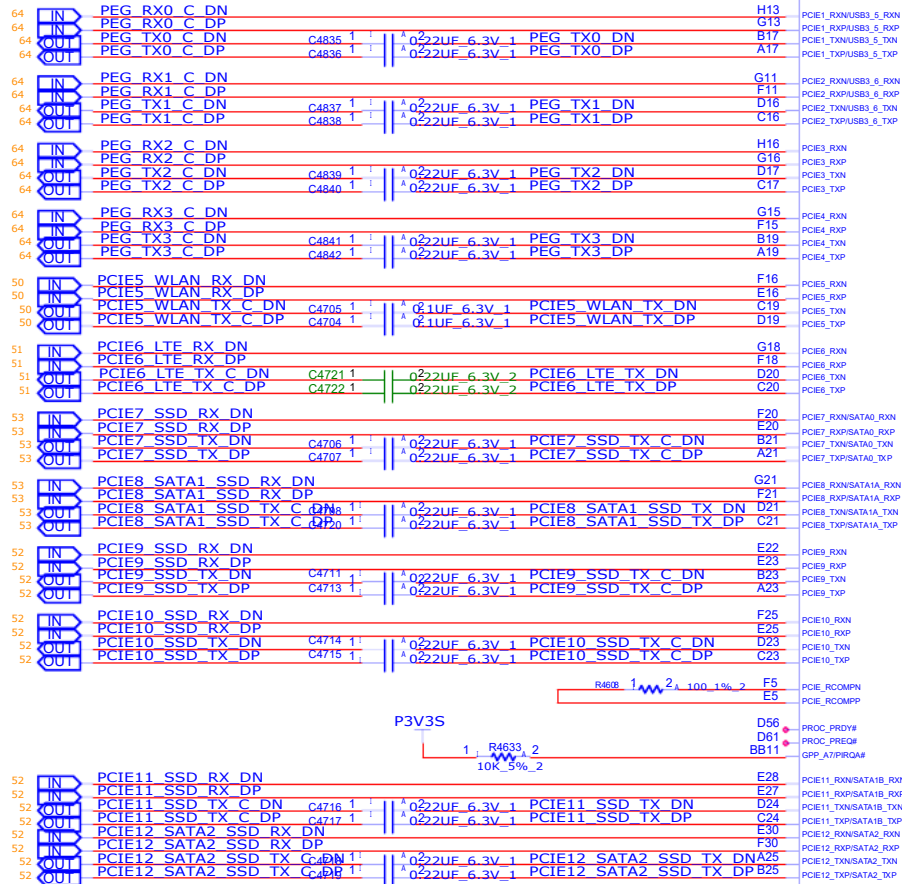
GPU

WLAN

LTE

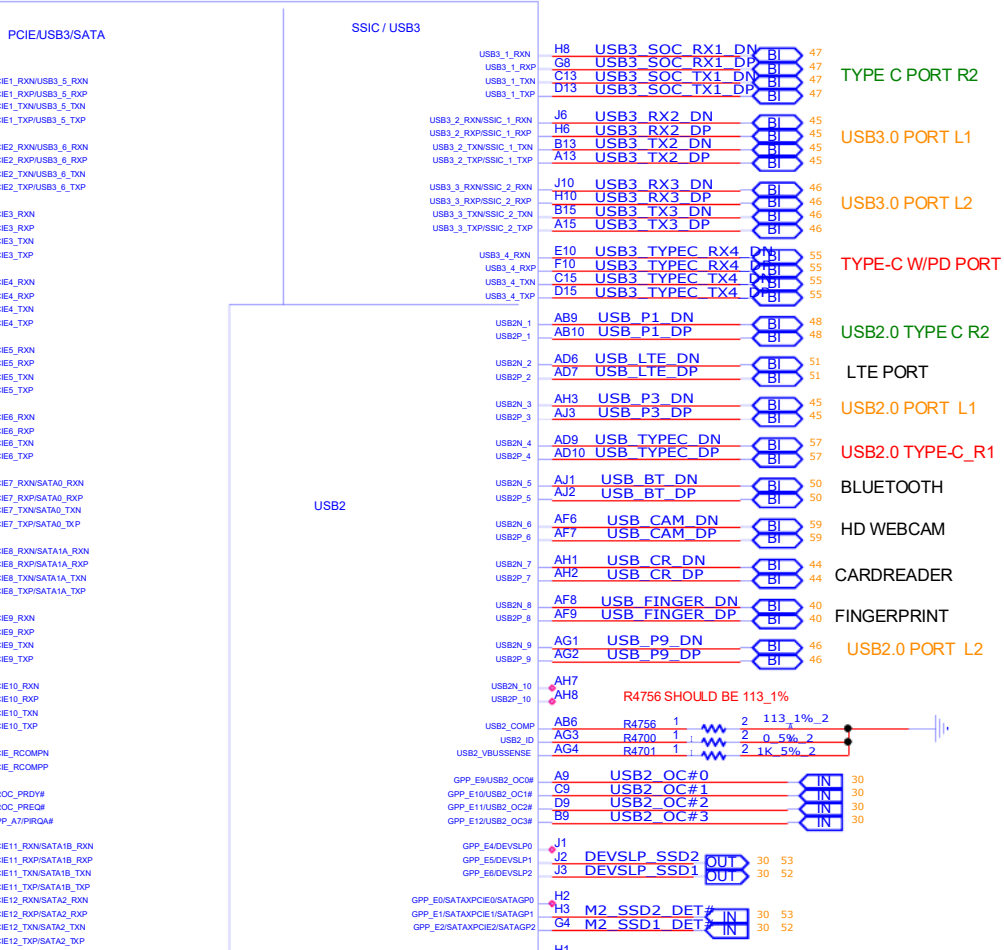
SSD 2X

SSD 4X



U4500

SKL_ULT



REFER PDG CHAPTER 36
DESIGN CONSTRAINT: FOR PCIe® GEN 3/ SATA MULTIPLEXED CONFIGURATION, MOTHERBOARD TX REQUIRES A 220 N
AC CAPACITOR AND NO AC CAPACITOR IS REQUIRED FOR MOTHERBOARD RX CHANNEL

INTEL_H23951_BGA_1356P

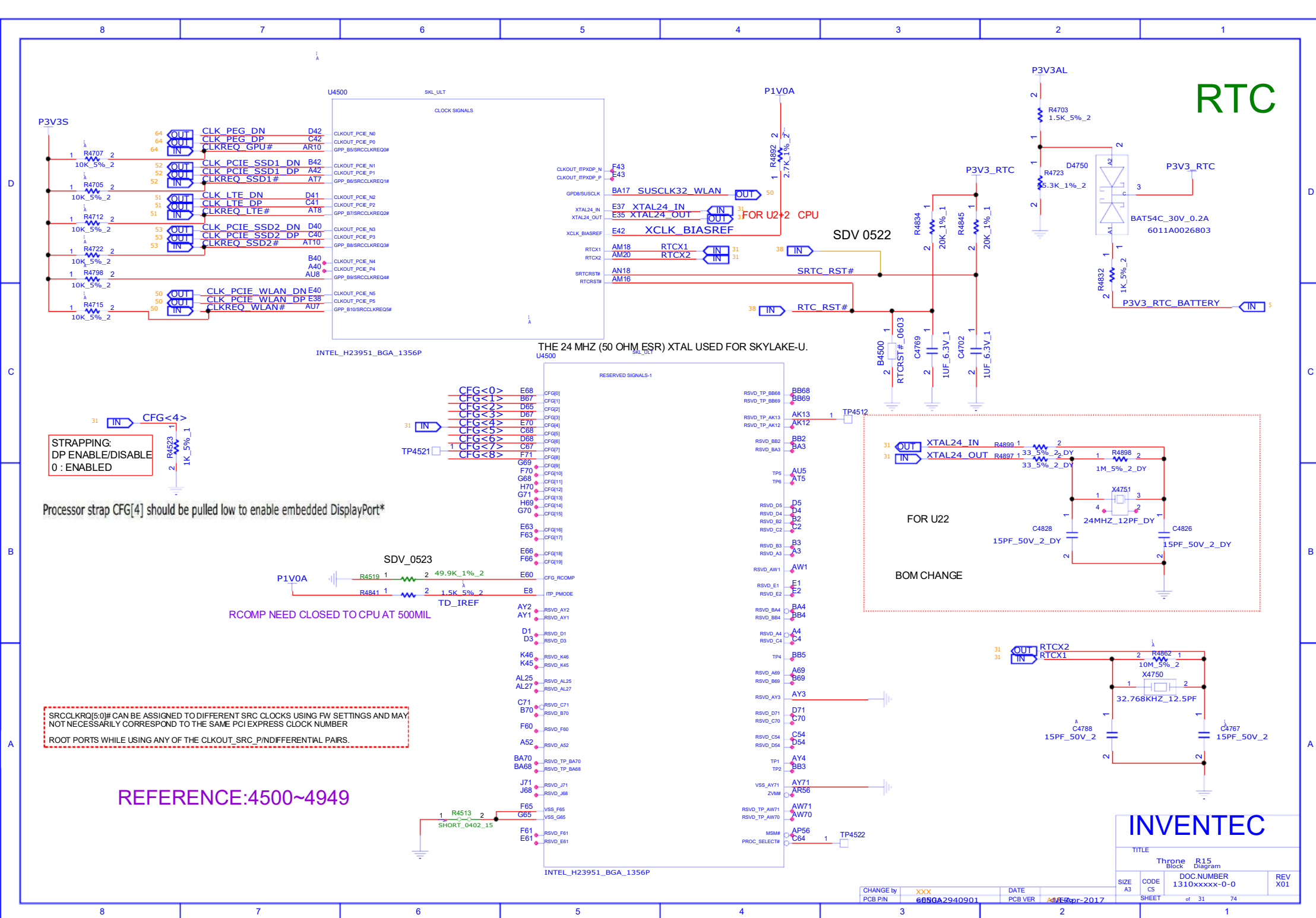
INVENTEC

TITLE
Throne R15 Block Diagram

SIZE A3 CODE CS DOCNUMBER 1310xxxxx-0-0 REV X01

CHANGE BY XING> 6050A2940901 DATE 18-Apr-2017 PCB VER A0000>

SHEET 30 of 74



D

C

B

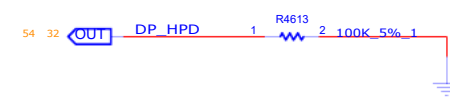
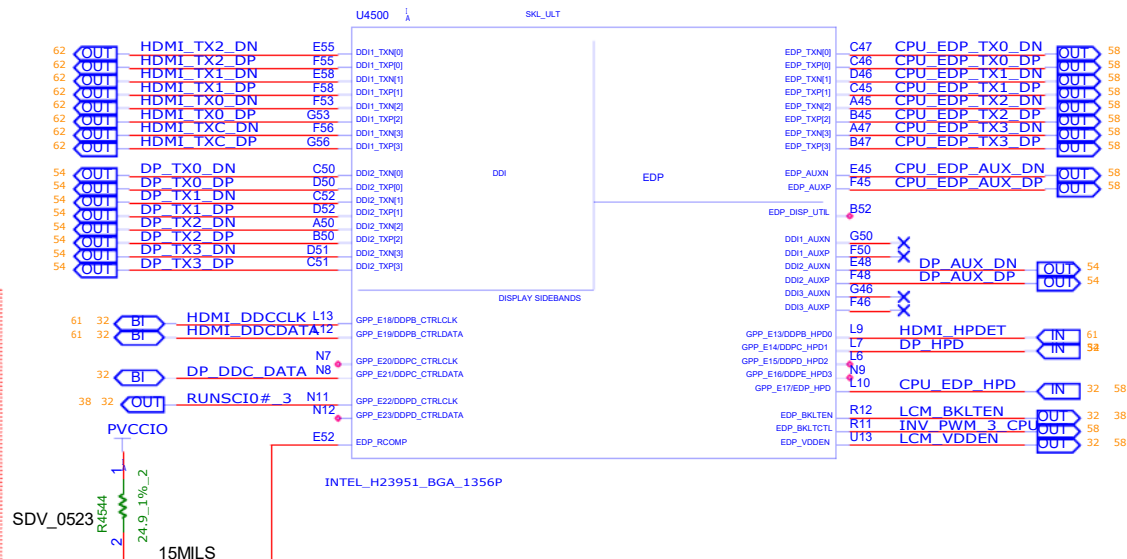
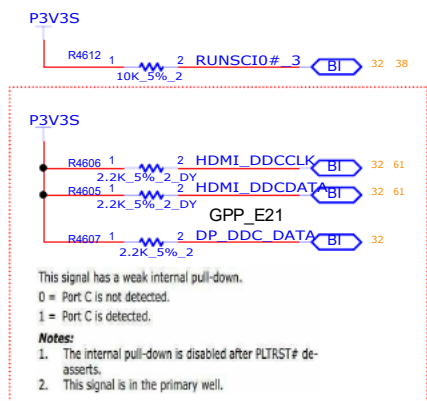
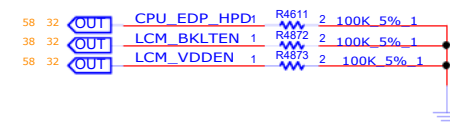
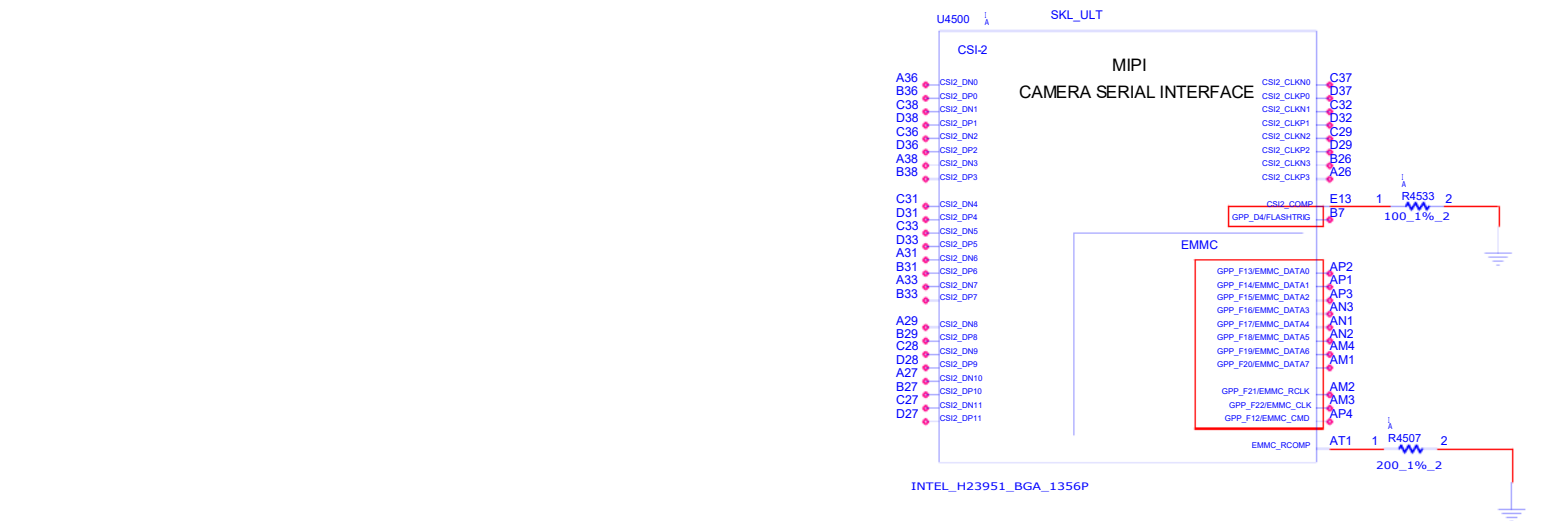
A

D

C

B

A



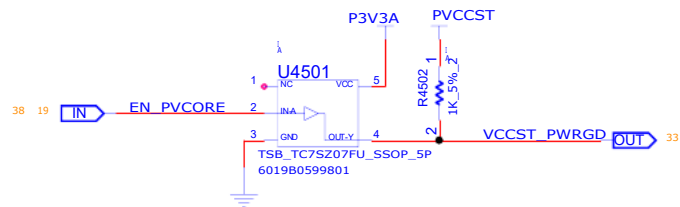
INVENTEC

TITLE
Throne R15
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

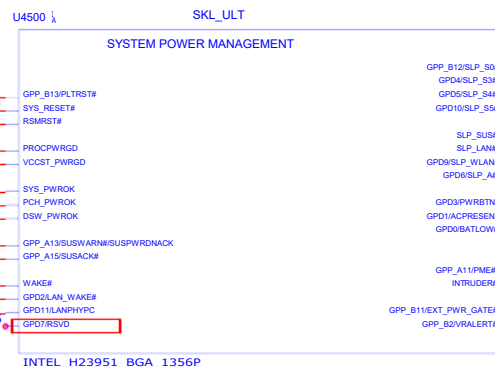
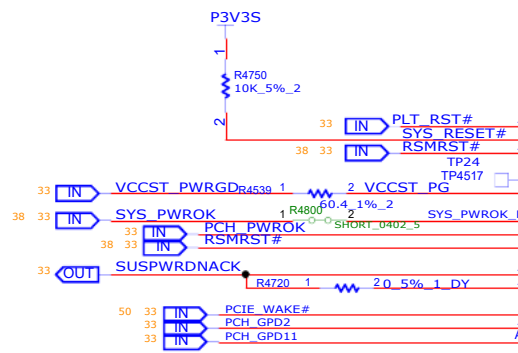
CHANGE by PCB P/N	X<ENG> 6050A2940901	DATE PCB VER	18-Apr-2017 A0/VER>
----------------------	------------------------	-----------------	------------------------

SHEET 32 of 74

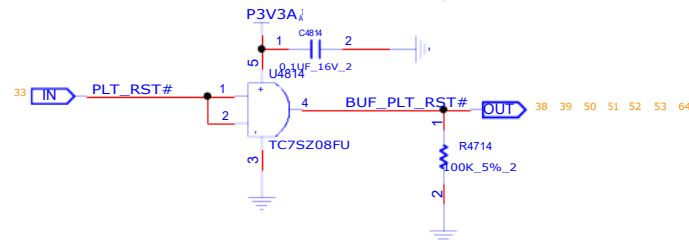
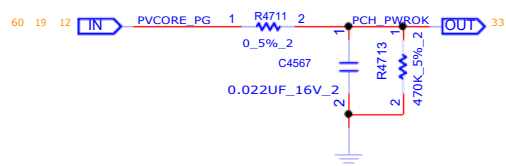
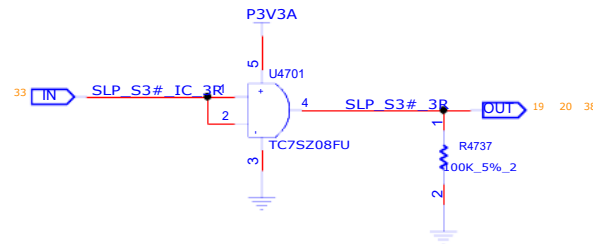
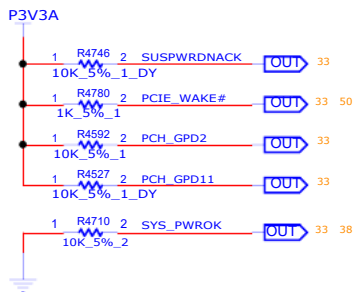
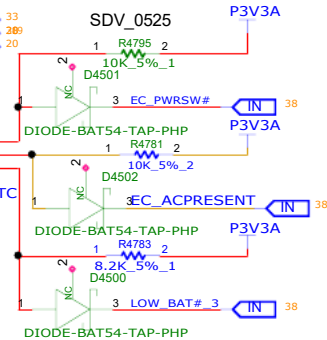


PCH Power OK: When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable for at least 5 ms. PCH_PWROK can be driven asynchronously. When PCH_PWROK is negated, the PCH asserts PLTRST#.

Note: PCH_PWROK must not glitch, even if RSMRST# is low.



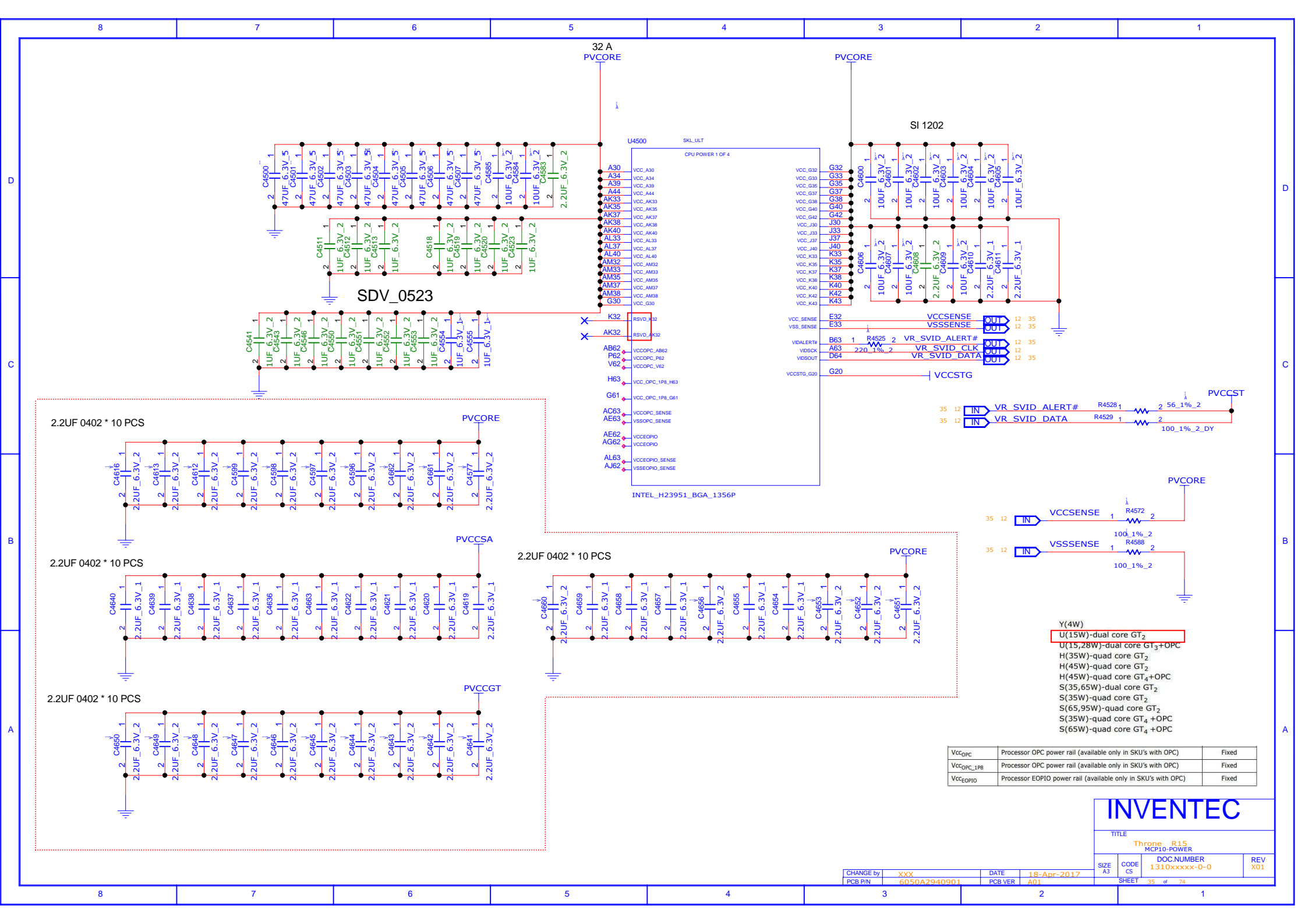
SLP_# output signal can be used to cut power to the Intel Management Engine and SPI flash on a platform that supports the M3 state (for example, certain power policies in Intel AMT).



INVENTEC

TITLE			
Throne R15 Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		33 of 74	

CHANGE by	XENG>	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	ADVER>



VCCOPC	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCOPC_LPB	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCEOPIO	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

INVENTEC

TITLE			
Throne_R15 MCP10-POWER			
SIZE A3	CODE CS	DOCNUMBER 1310xxxxx-0-0	REV X01
SHEET 35 of 74			

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

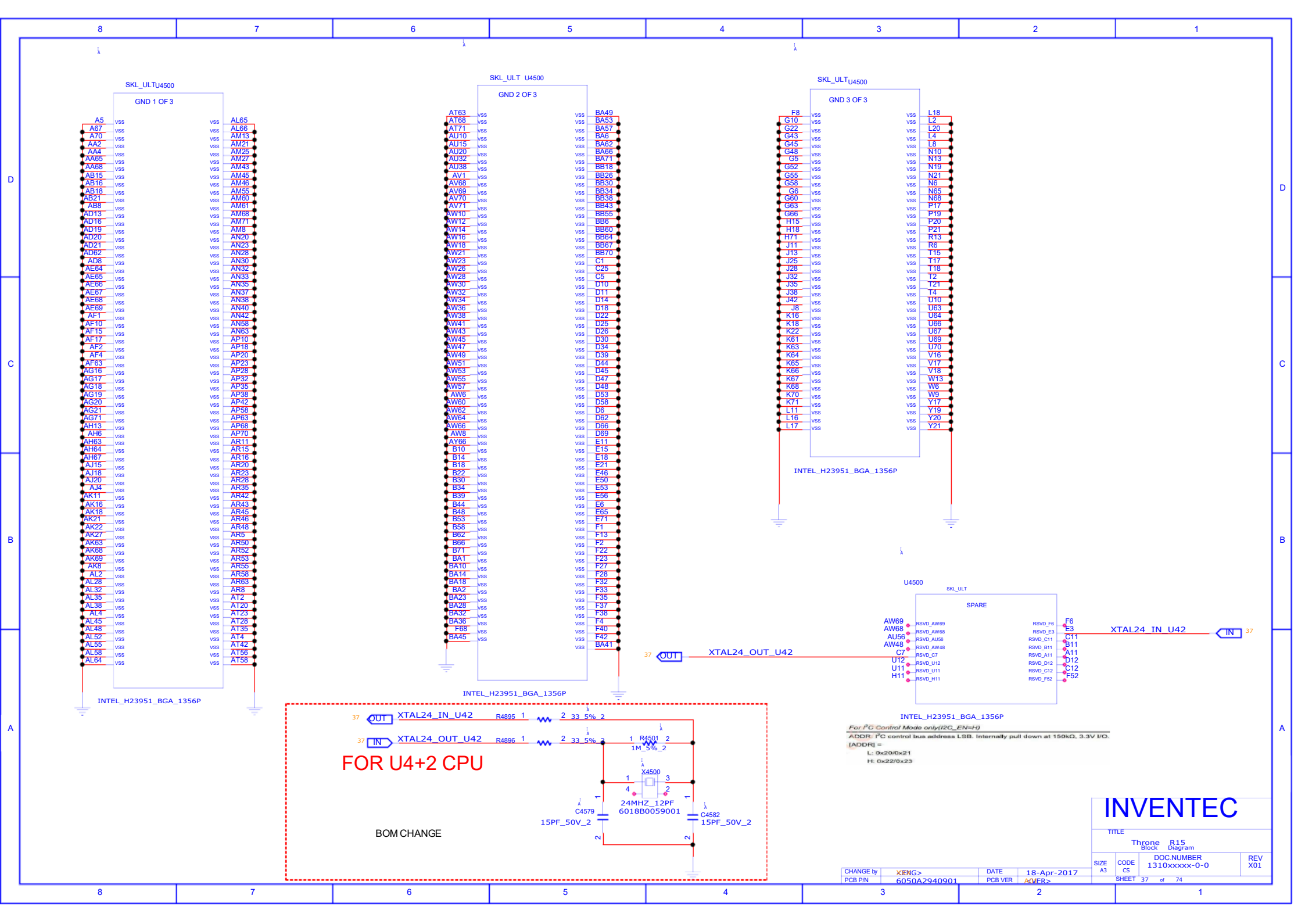


Vcc _{GTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
--------------------	---	------

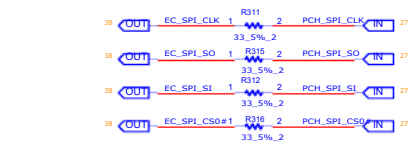
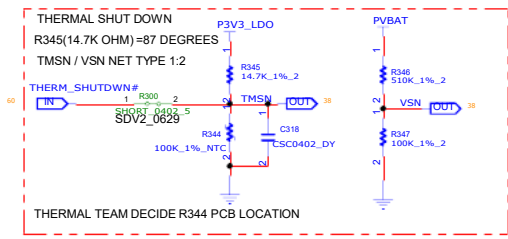
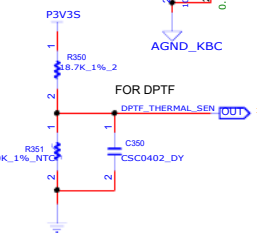
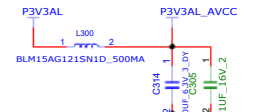
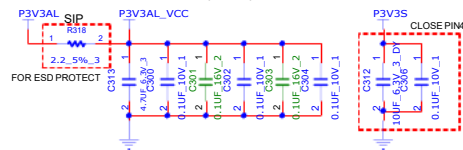
TITLE
Throne R15

SIZE	CODE	DOC.NUMBER
------	------	------------

CHANGE by	XXX	DATE	18-Apr-2017	SIZE	CODE	1310xxxxx-0-0
PCB P/N	6050A2940901	PCB VER	A01	A3	CS	
				SHEET	36	of 74

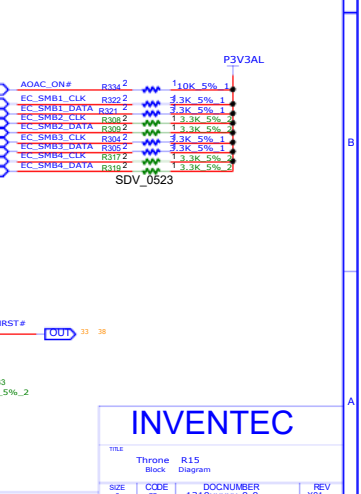
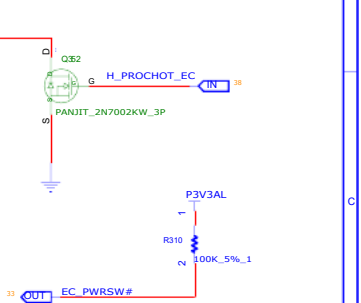
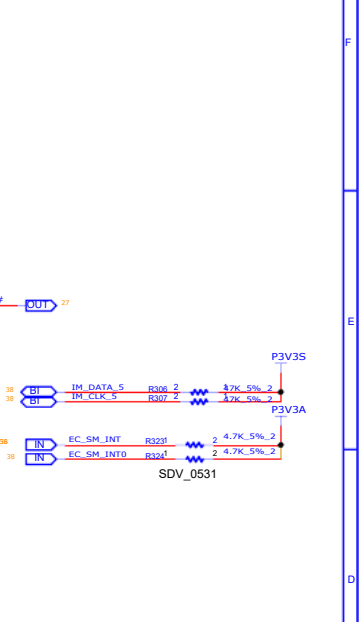
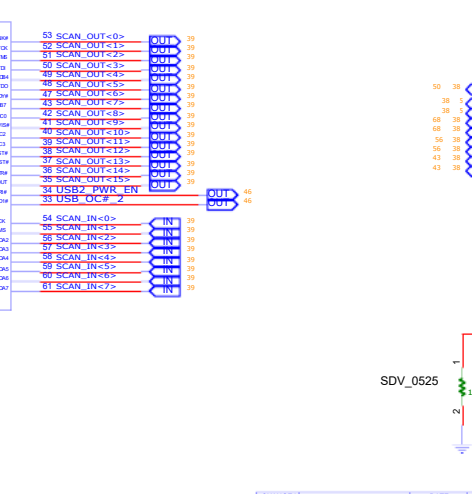
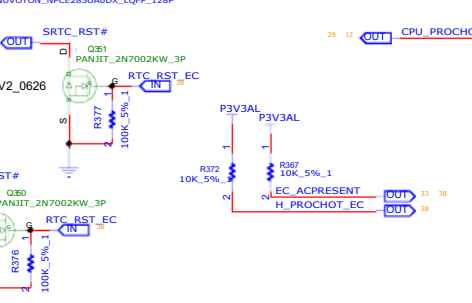
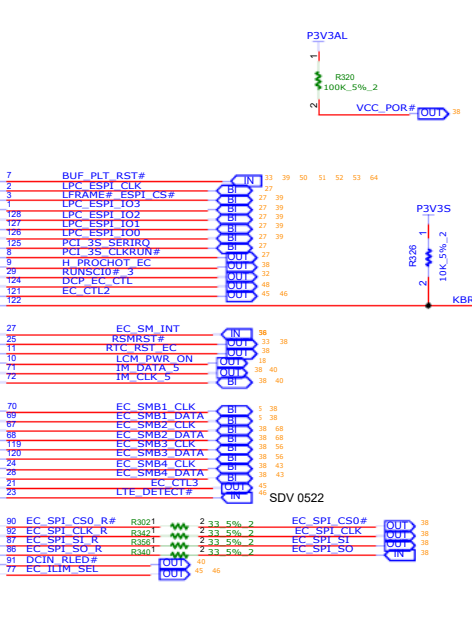
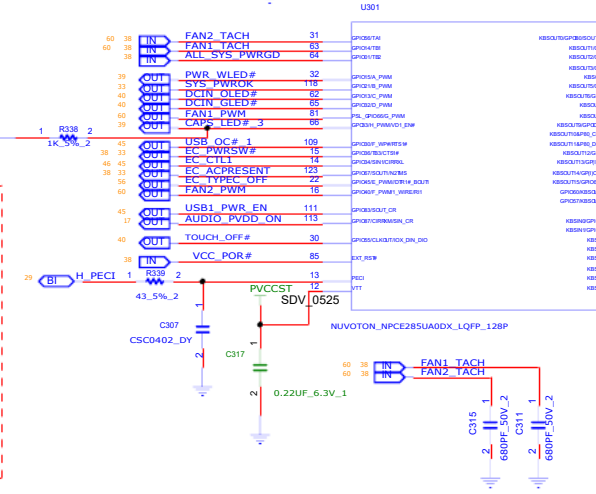
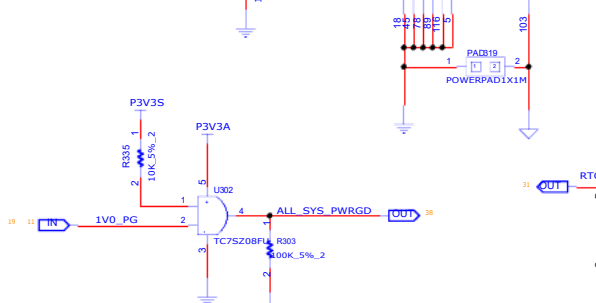
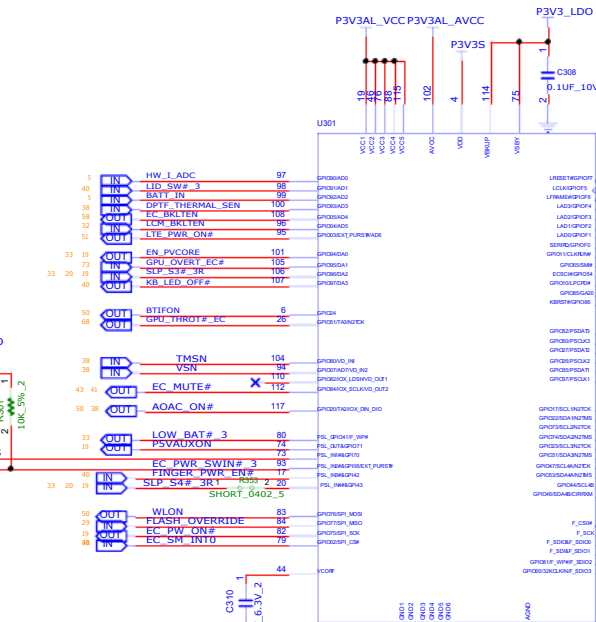
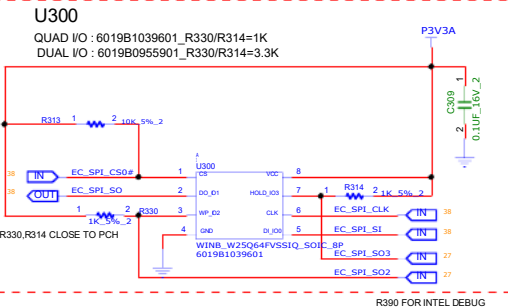


REFERENCE 300-389(KBC)



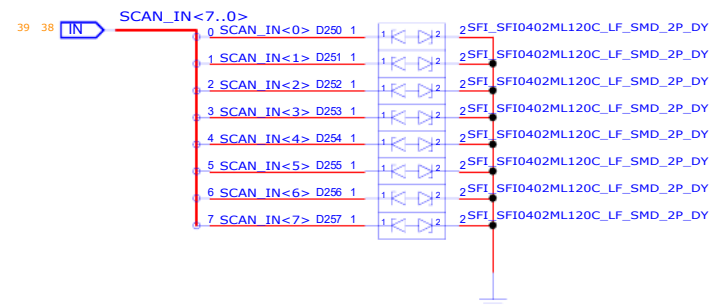
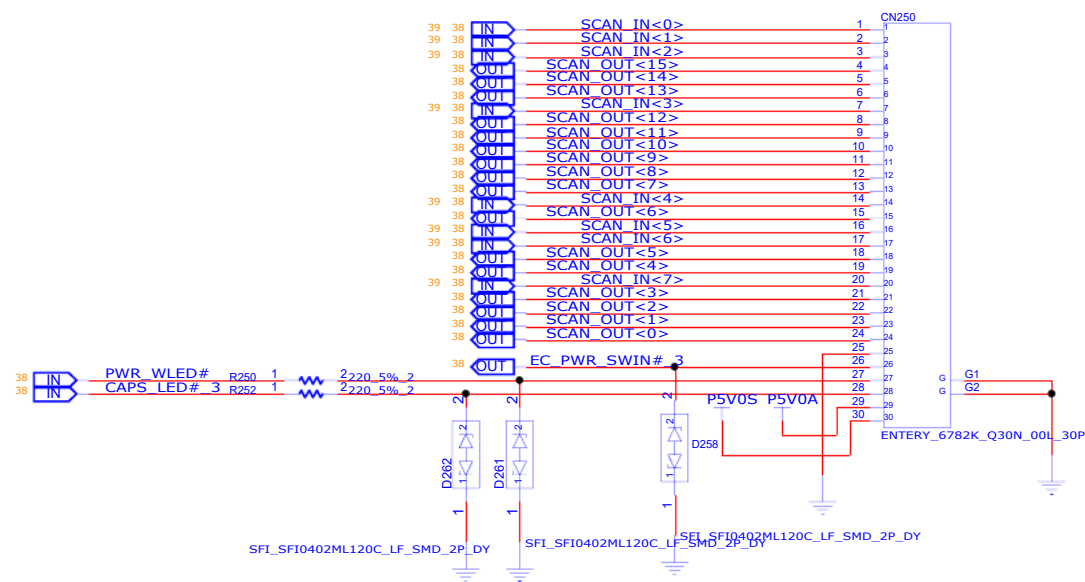
EC_SMB1	EC_SMB2	EC_SMB3	EC_SMB4
1.BATTERY	USB3 HUB	TYPE C	TI AMP
2.CHARGE	GPU	TYPE C P1	

ALL EC & PCH RESISTOR NEED TO WITHIN 0.5" OF ROM(U300)

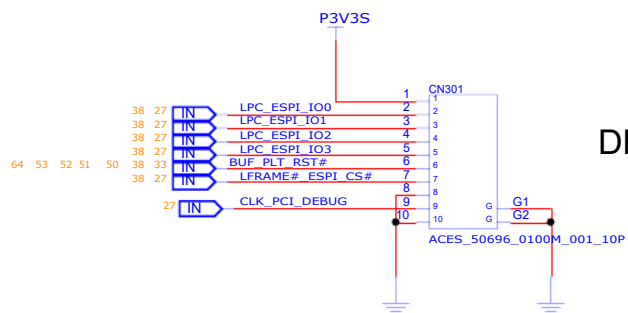


INVENTEC

KEYBOARD CONN



DEBUG CONN

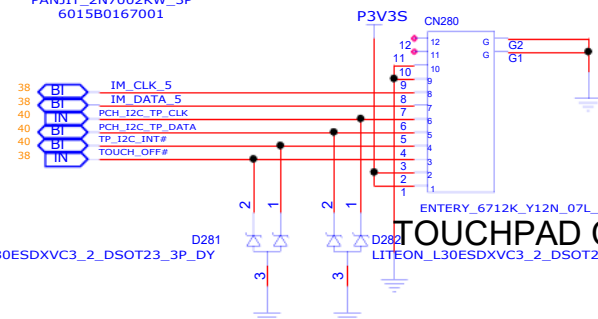
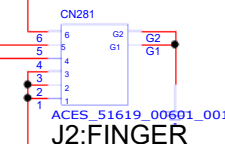
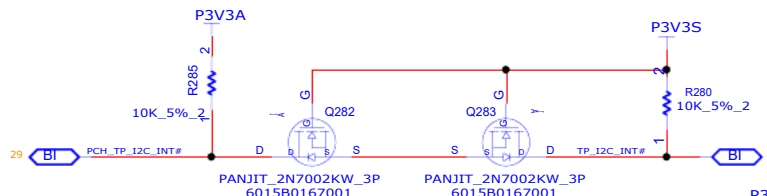
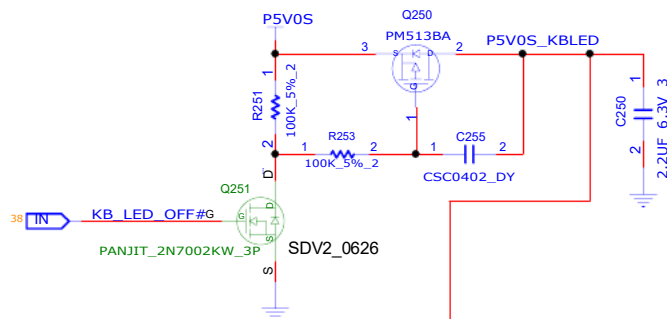
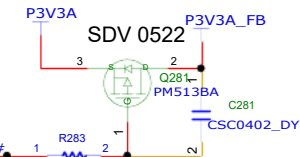
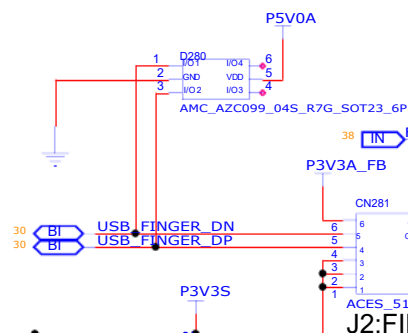
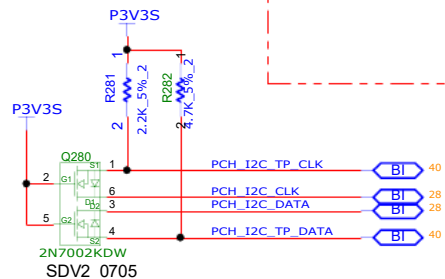
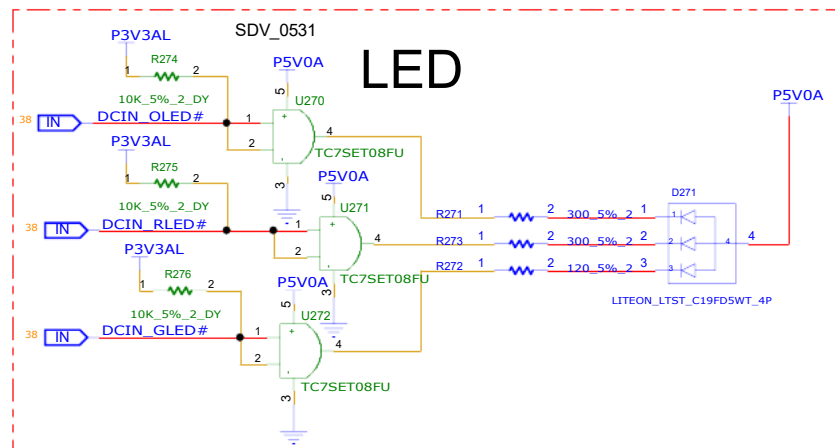
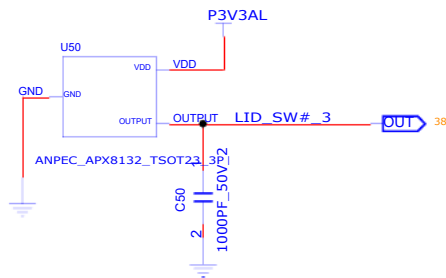


INVENTEC

TITLE
Throne Block R15 Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		of 39	74

CHANGE by	XXX	DATE	
PCB P/N	6ENGA2940901	PCB VER	A08-Apr-2017



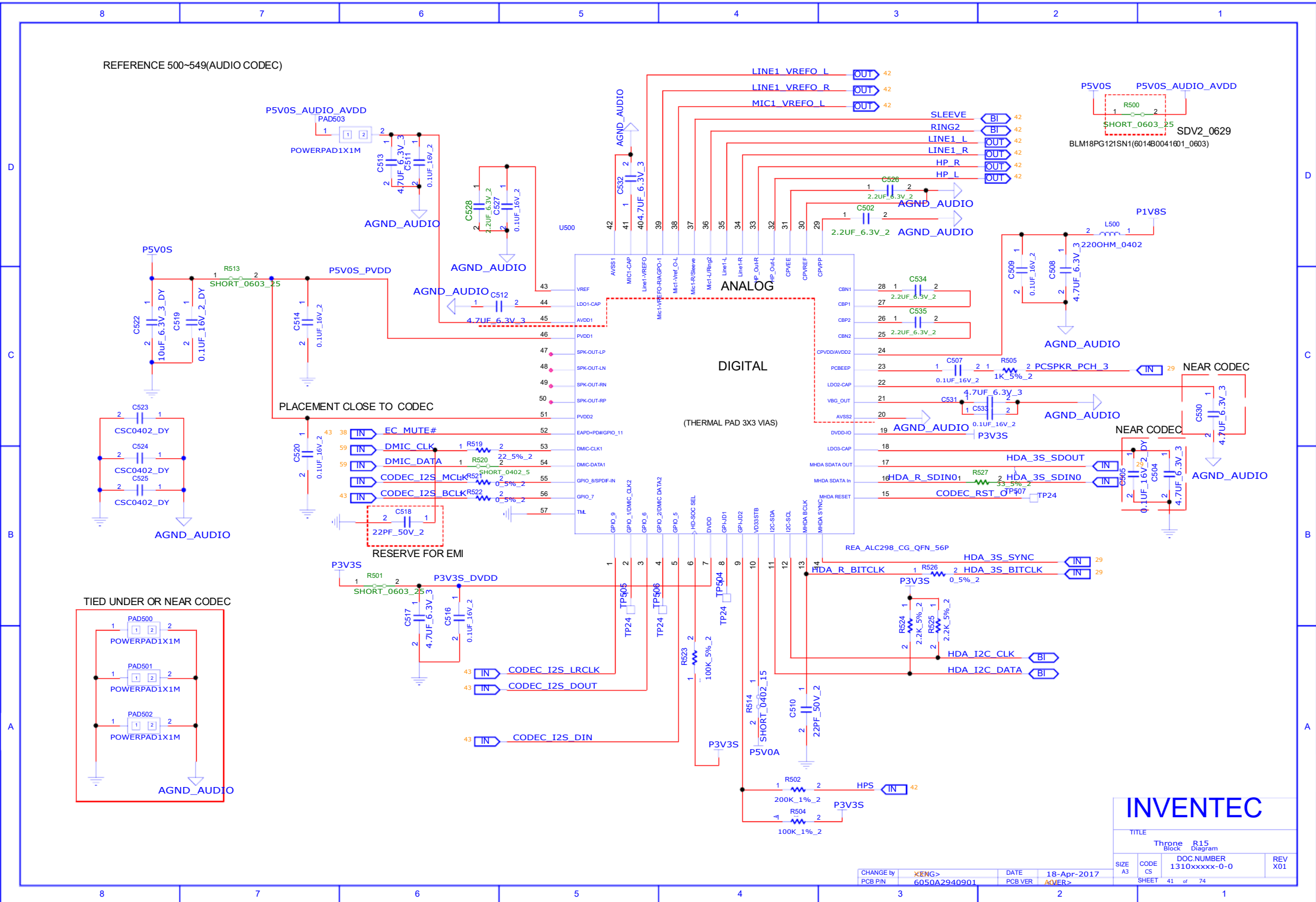
KEYBOARD LED CONN

TOUCHPAD CONN (CLICK PAD)

INVENTEC

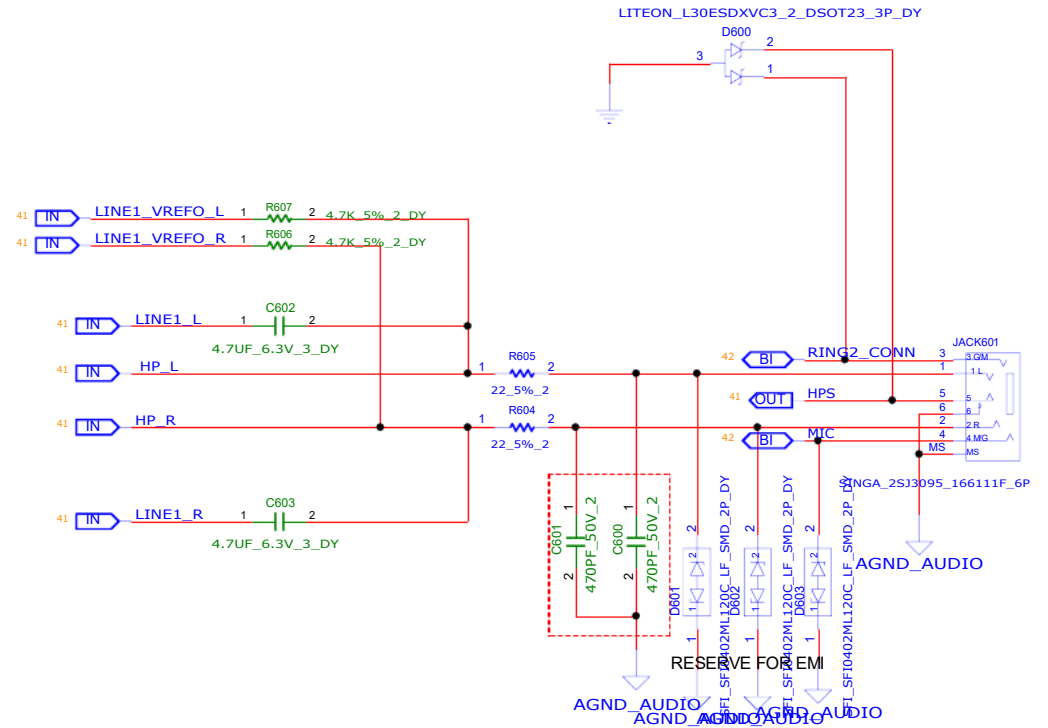
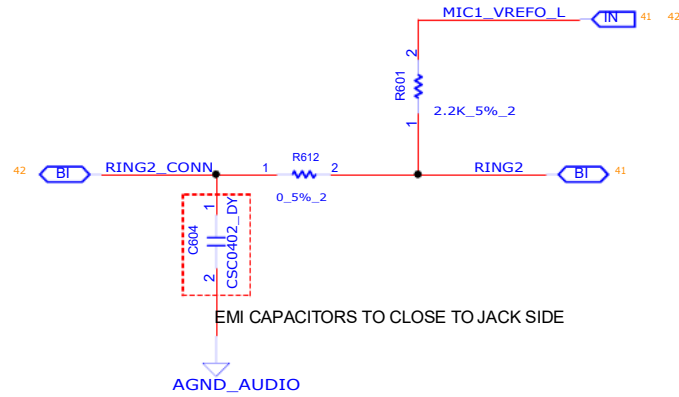
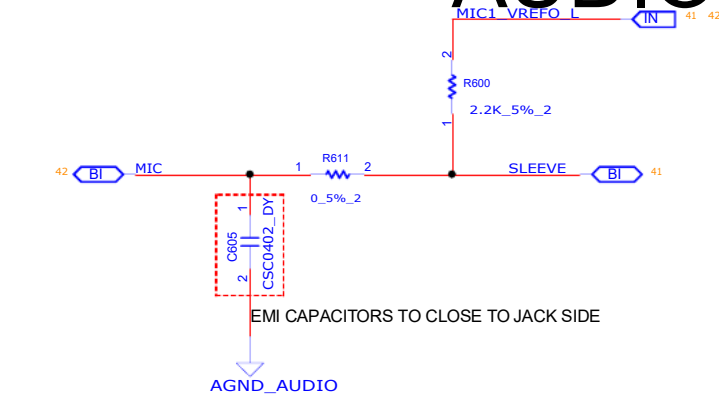
CHANGE by	XXX	DATE	18-Apr-2017
PCB PIN	6050A2940901	PCB VER	A01

TITLE	Throne R15 Block Diagram
SIZE	A3
CODE	CS
DOC NUMBER	1310xxxx-0-0
REV	X01
SHEET	40 of 74



REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



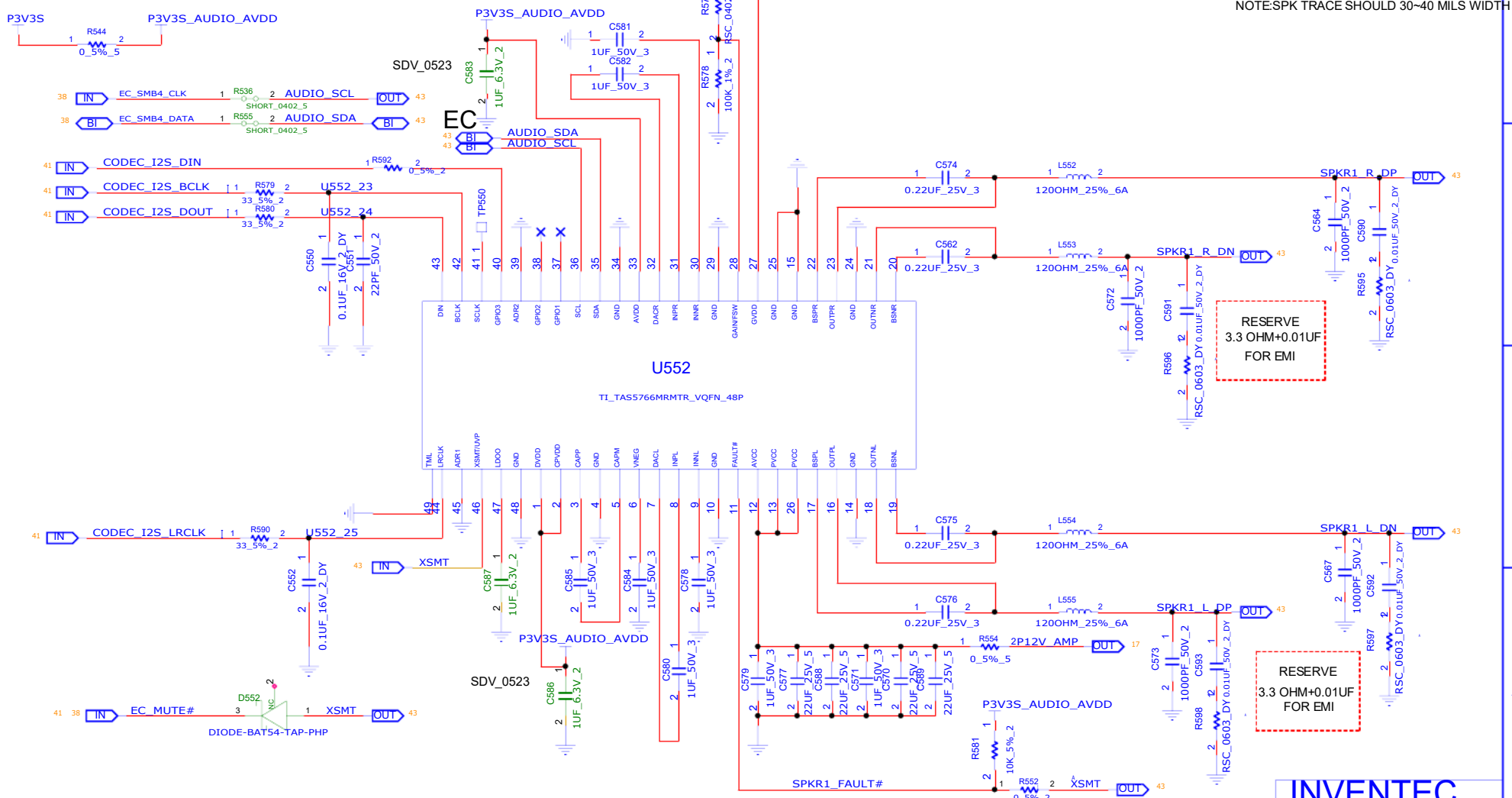
INVENTEC

TITLE			
Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 42 of 74			

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

INTERNAL SPEAKERS

NOTE:SPK TRACE SHOULD 30~40 MILS WIDTH



INVENTEC

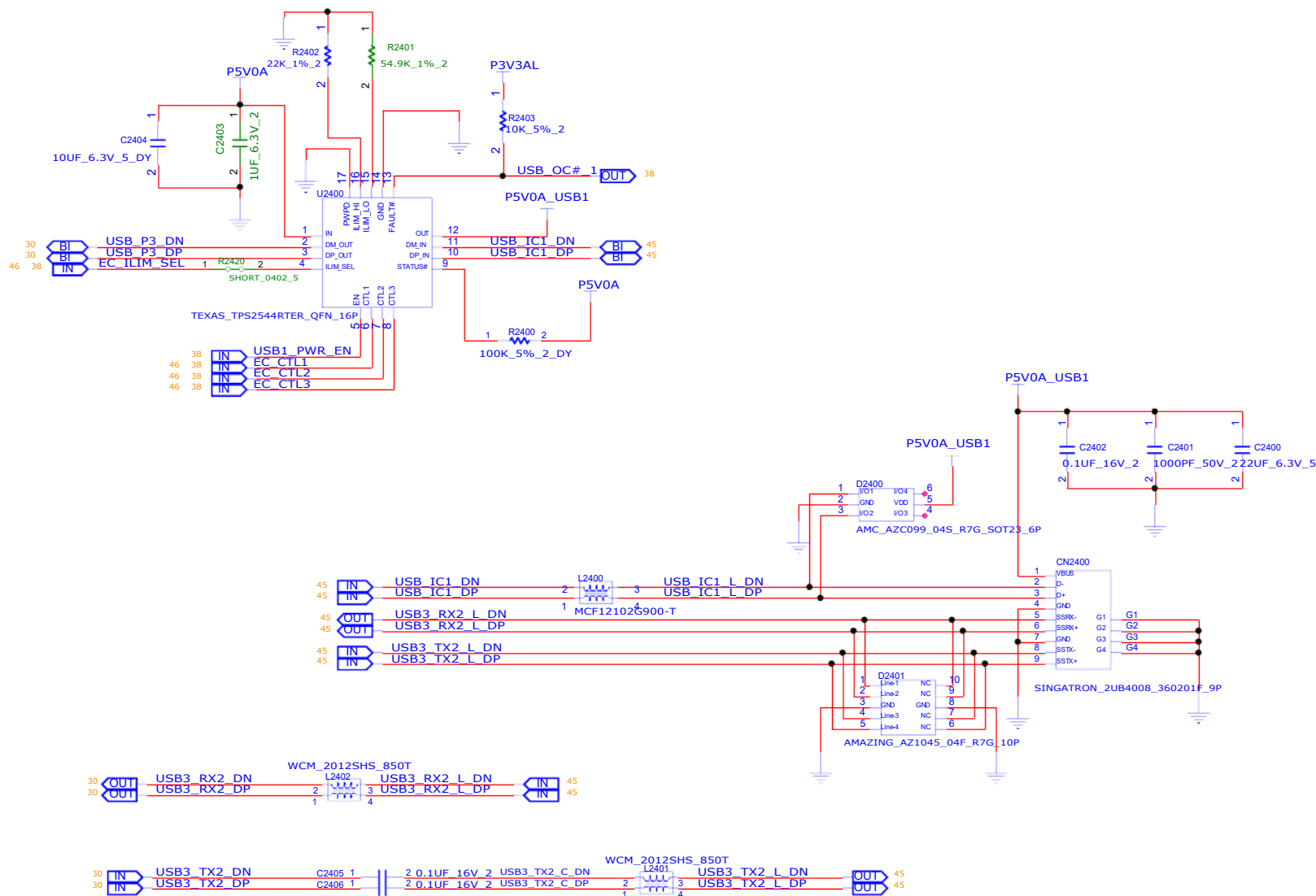
CHANGE by	XXX	DATE	18-Apr-2017	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	6050A2940901	PCB VER	A01			SHEET	43	of 74	



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		44 of 74	

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



INVENTEC

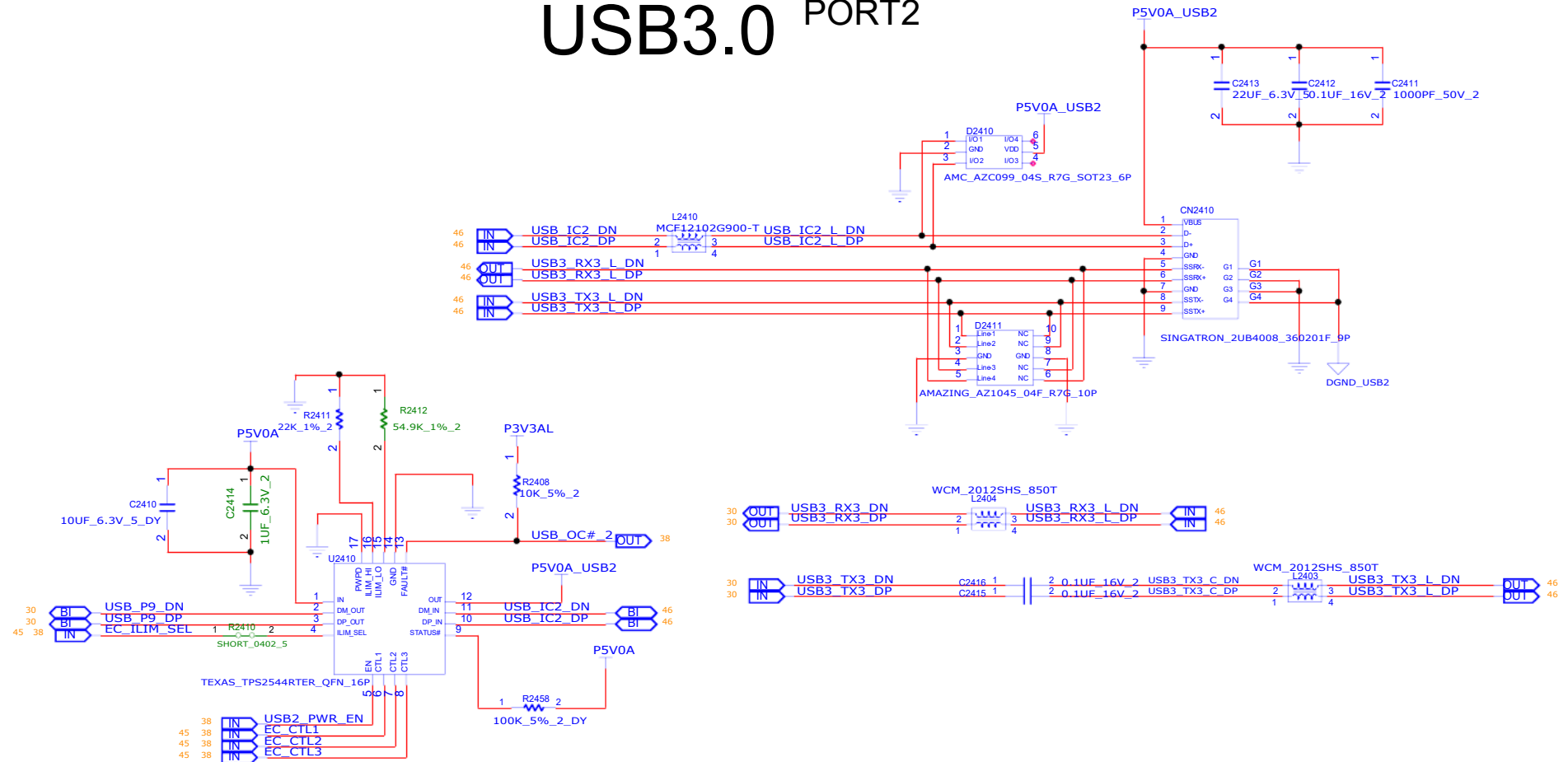
TITILE
Throne R15
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 18-Apr-2017
PCB P/N 6050A2940901 PCB VER A01

SHEET 45 of 74

USB3.0 PORT2



INVENTEC

TITLE			
Throne		R15	
Block		Diagram	
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	46	of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

REFERENCE 2600~2699(USB RESERVE)



TITLE

Throne Block R15 Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		47 of 74	

A	B	C	D	E	F
---	---	---	---	---	---

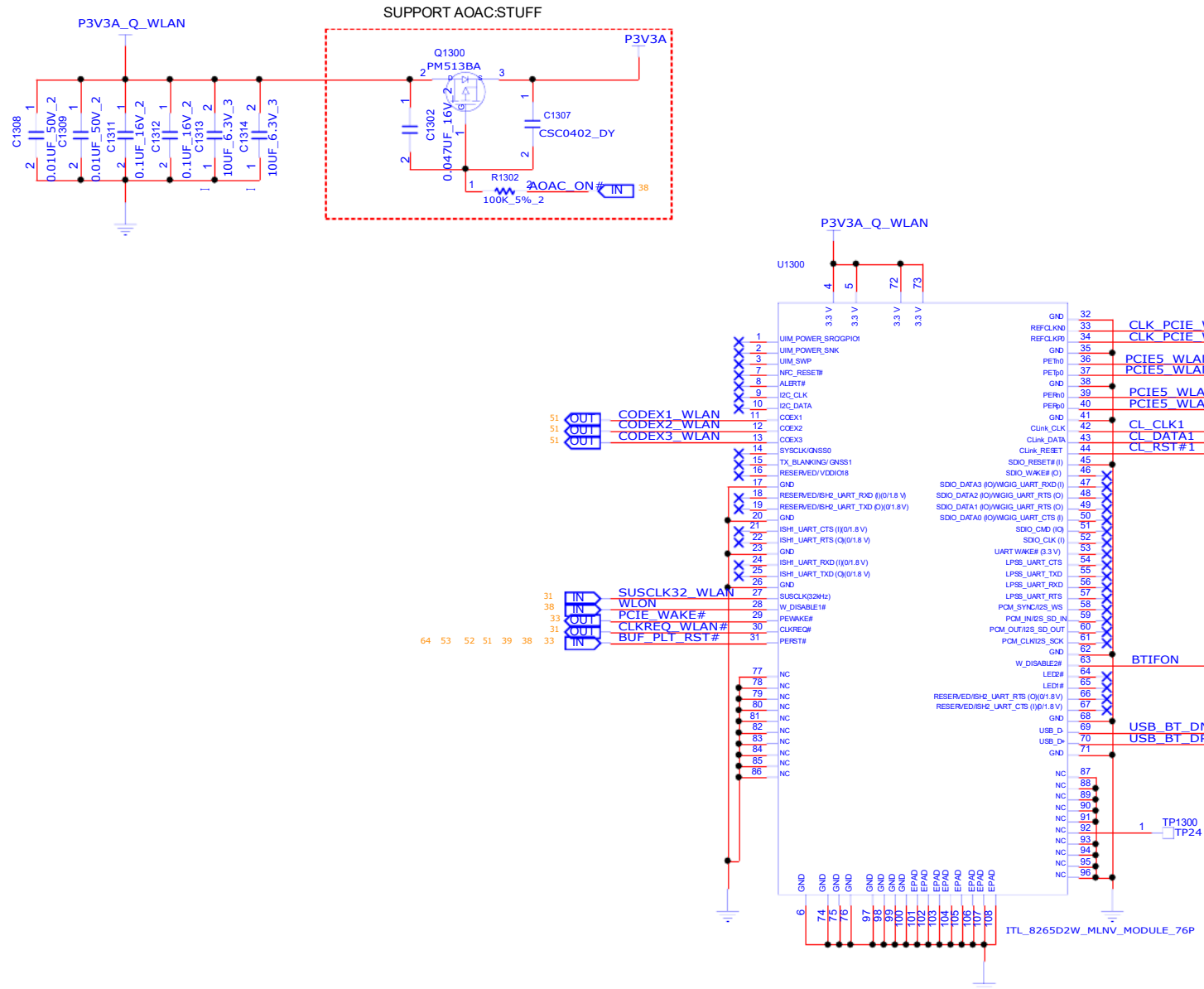
A	B	C
---	---	---

AA

A

B

WLAN
REFERENCE 1300 ~ 1349



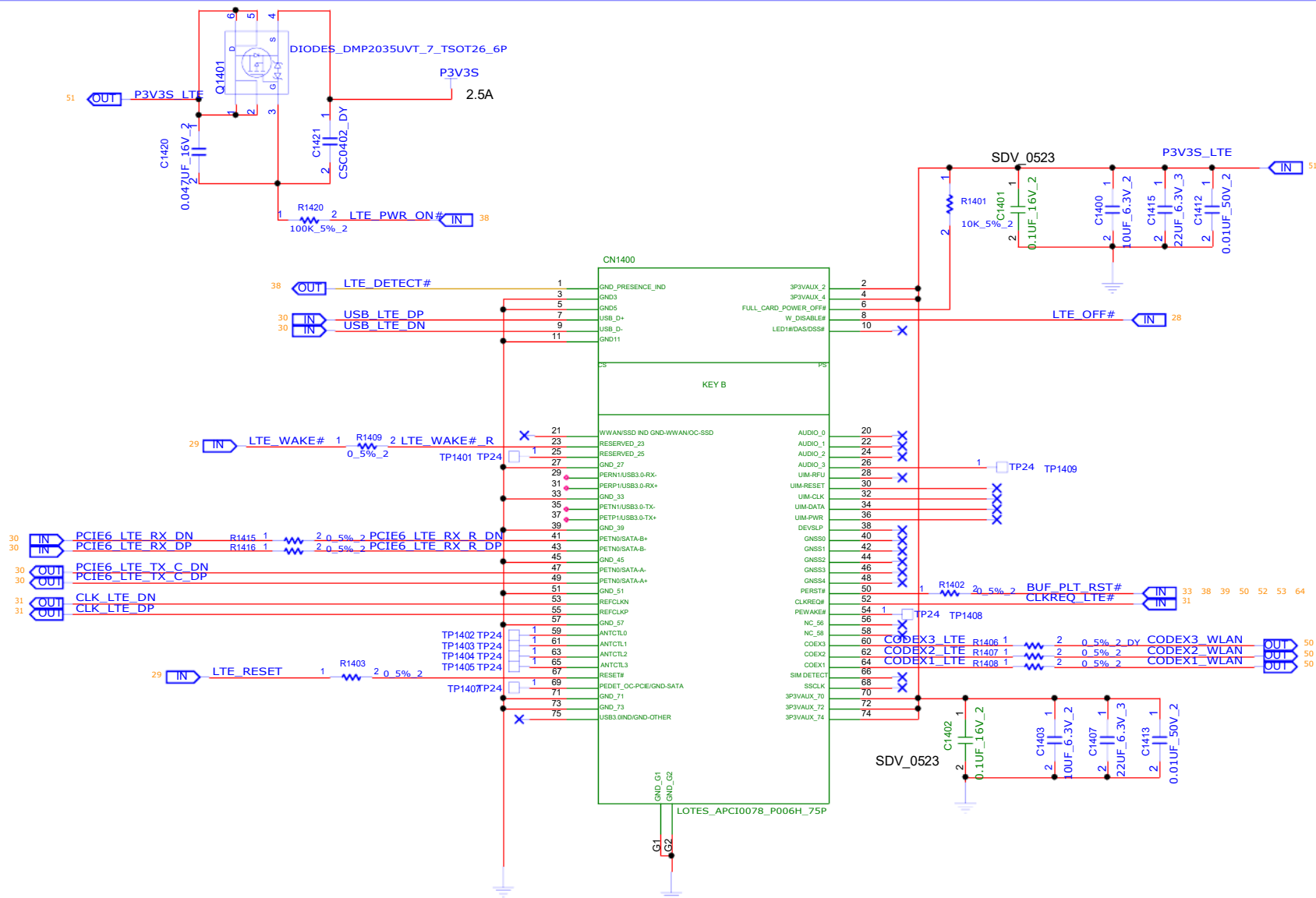
INVENTEC

TITLE			
Throne R15 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 50	of 74		

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

4G_LTE

REFERENCE 1400~1499(4G)

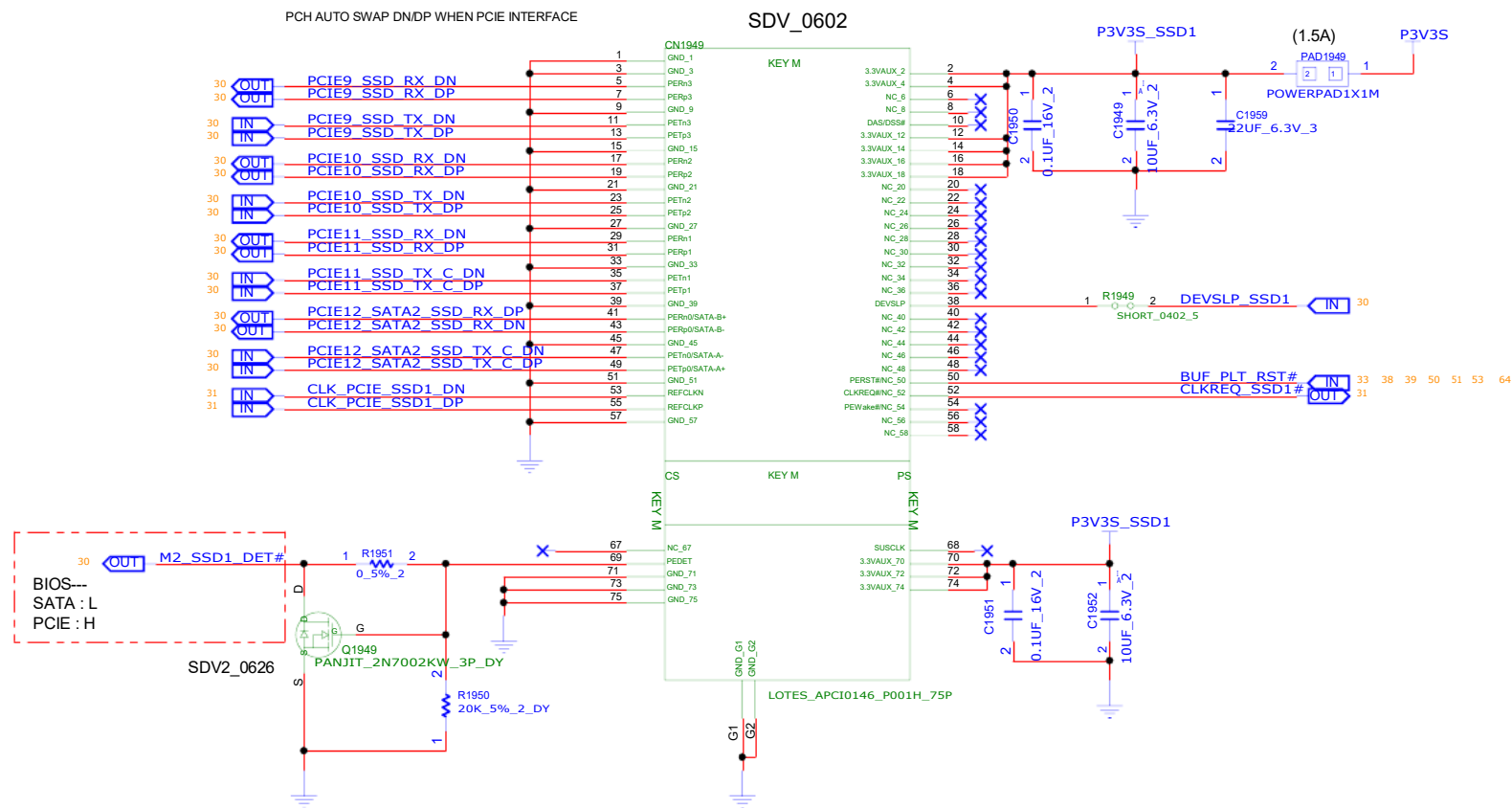


INVENTEC

TITLE			
Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	
SHEET	of 51	74	REV X01

CHANGE by	XXX	DATE	
PCB P/N	6RNGA2940901	PCB VER	A18-Apr-2017

NGFF SSD1(PCIe/SATA 4X)



INVENTEC

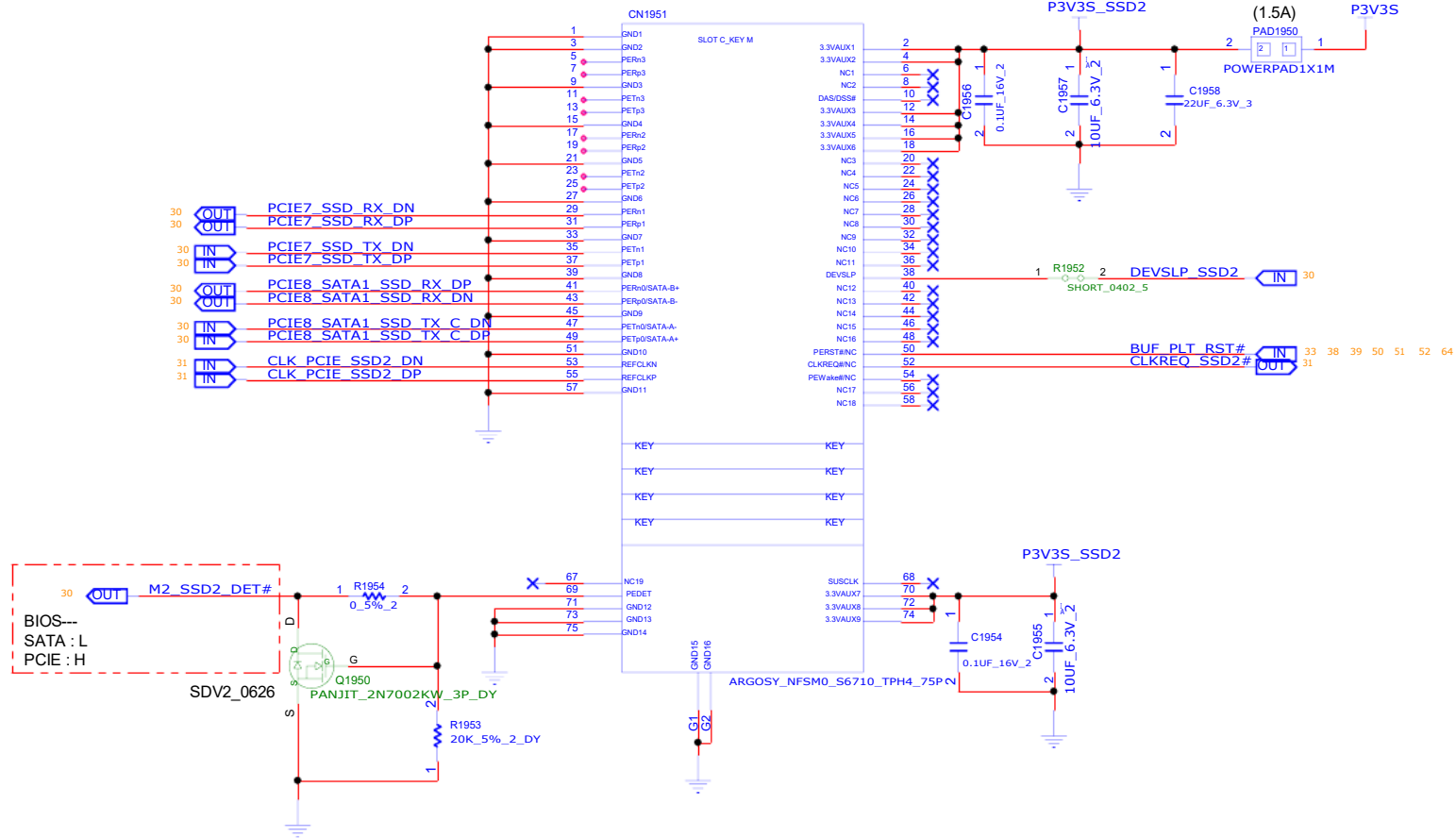
TITLE
Throne Block R15 Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET		52 of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

NGFF SSD2(PCIE/SATA 2X)

PCH AUTO SWAP DN/DP WHEN PCIE INTERFACE



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

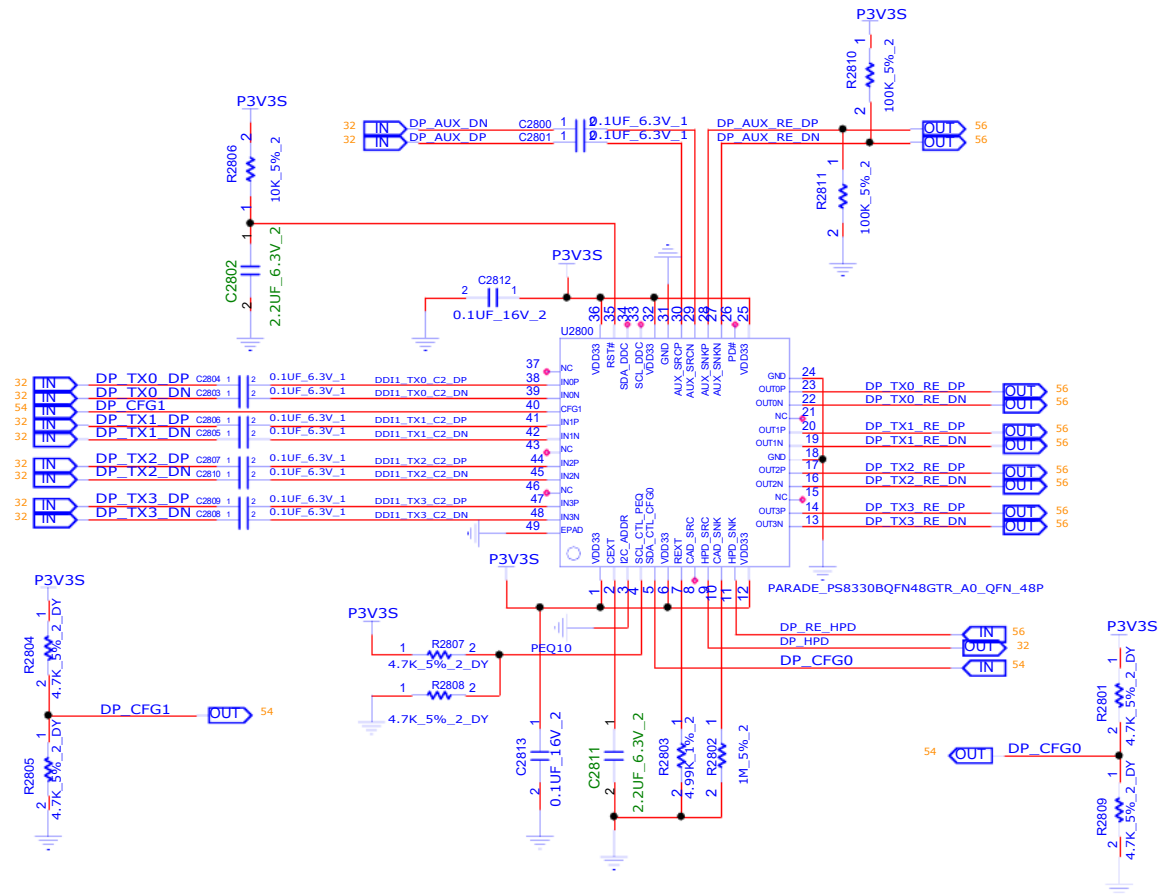
REFERENCE NUMBER:1950~1999

INVENTEC

TITLE			
Throne Block R15 Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	53	of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

DP REDRIVER



INVENTEC

TITLE			
Throne Block		R15 Diagram	
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 54	of 74		

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

3.3V MODE	5V MODE
R2602	V OPEN
R2698	OPEN V
Q2691	OPEN V
R2600	V OPEN

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

Truth Table

SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M+
H	L	D+	D+

INVENTEC

TITLE	Throne R15
SIZE	TP55450
CODE	1310xxxx-0-0
REV	X01
SHEET	56 24

CHANGE BY XXXX DATE 18-Apr-2017 PCB PIN 6050A2940901 PCB VER AVER>

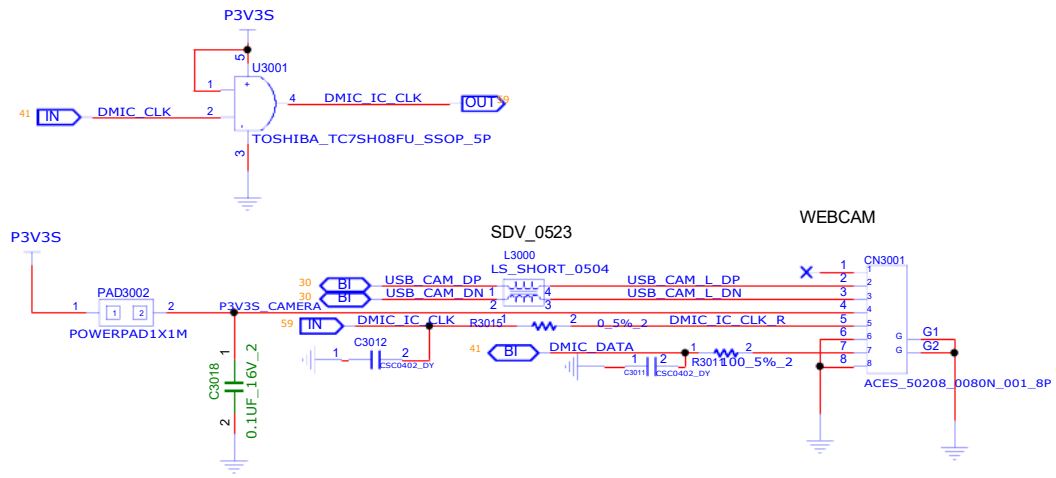
EDP CONN



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
SHEET		58 of 74

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

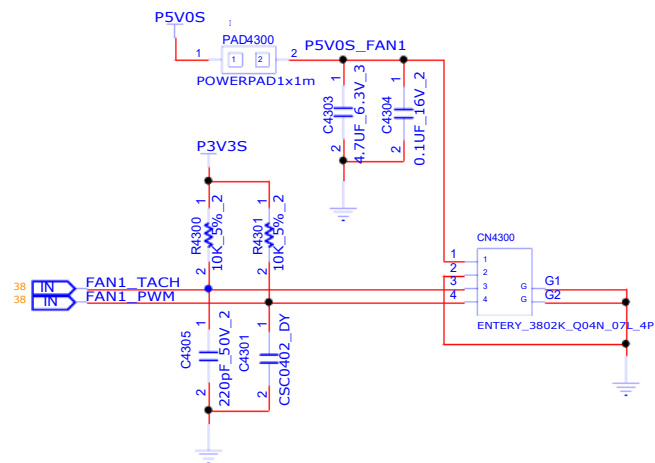
WEBCAM



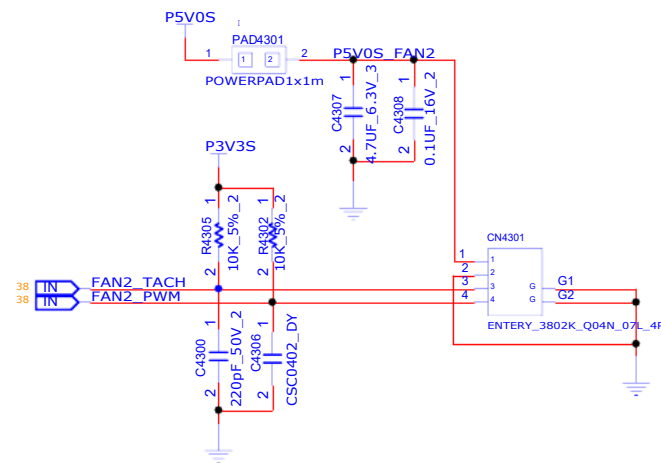
INVENTEC

CHANGE by		XXX	DATE		18-Apr-2017
PCB P/N		6050A2940901	PCB VER		A01
SIZE	A3	CODE	CS	DOC NUMBER	
SHEET	59	of	74	1310xxxxx-0-0	
				REV	X01

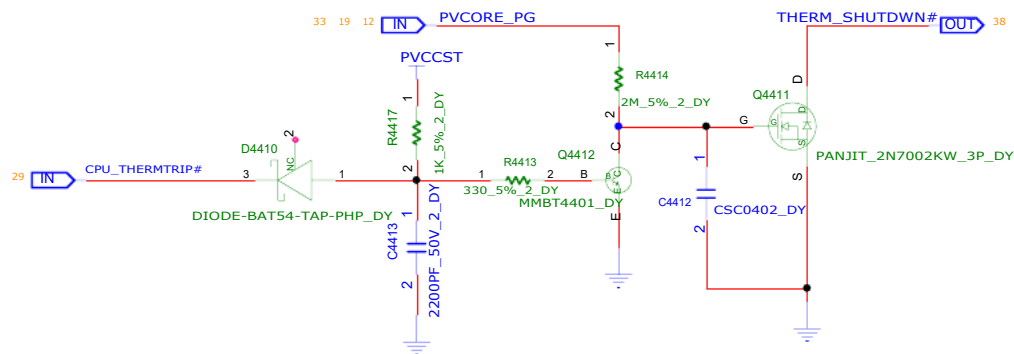
REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU



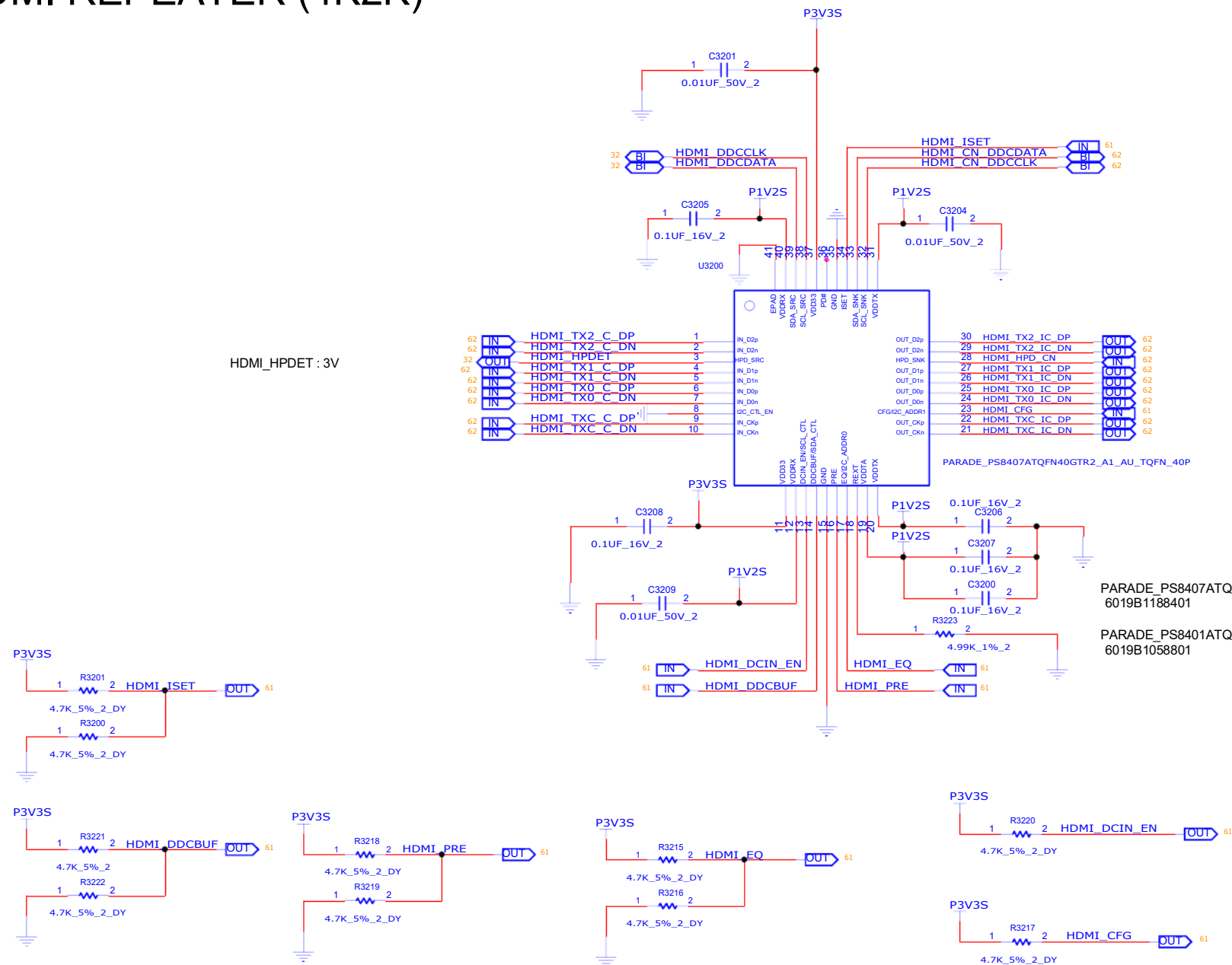
REFERENCE NUMBER:4411~4449

INVENTEC

CHANGE by XXX
PCB P/N 6P8GA2940901
DATE
PCB VER A18-Apr-2017

TITLE			
Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET	of 60	74	

HDMI REPEATER (4K2K)



INVENTEC

TITLE			
Throne Block R15 Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		61 of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

THIS DRAWING AND SPECIFICATIONS, HEREIN ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION, INVENTEC CORPORATION, ALL RIGHT RESERVED.

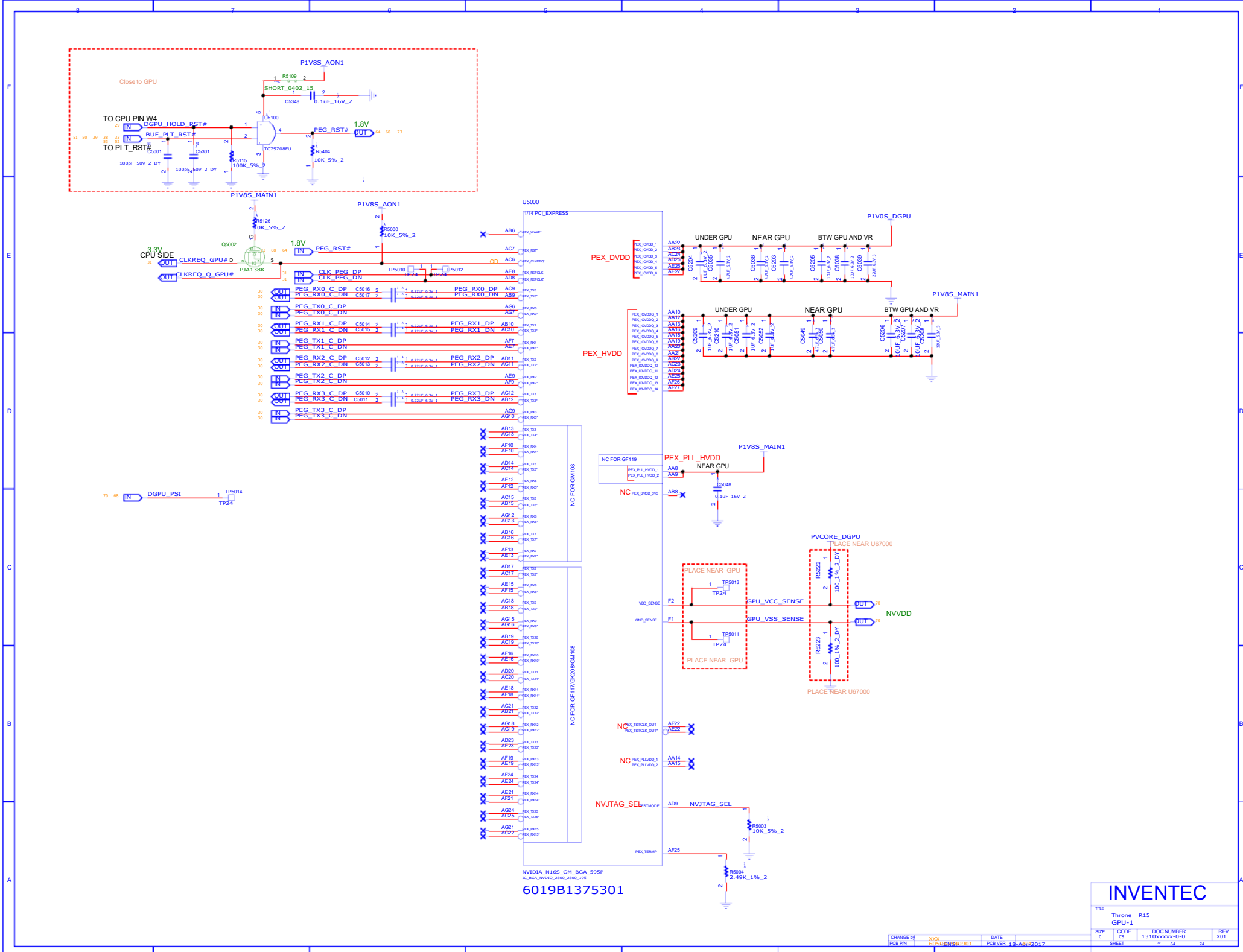
NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

N17S-LG
GDDR5 23X23

2017.08.09

18-Apr-2017		
DATE	CHANGE NO.	REV

Chun, Sheng Huang, Yeng			Shiu, Vini			INVENTEC			
DESIGN / DRAWER	XXX	DATE	18-Apr-2017	TITLE	Throne	R15			
CHECK				SIZE	A0		CLUE	DOC NUMBER	REV
APPROVAL				CS	1310xxxxx-0-0		X01		
FILE NAME	6866-1940501	PCB VER	A01	SHEET	of	63	24		



F
E
D
C
B
A

IC: RGA_NV030_2300_2300_195
U5000

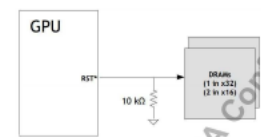
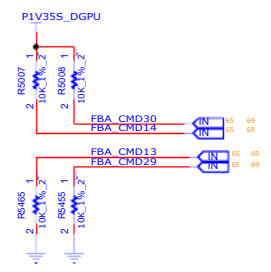
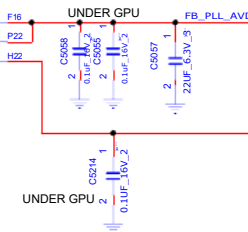
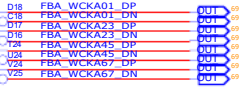
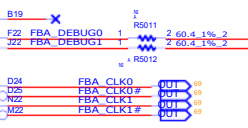
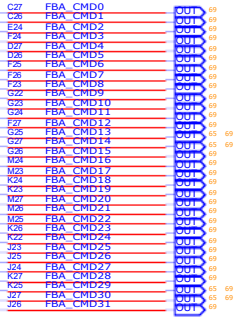
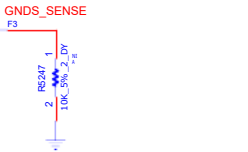
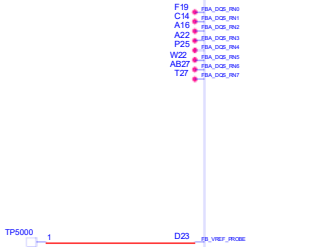
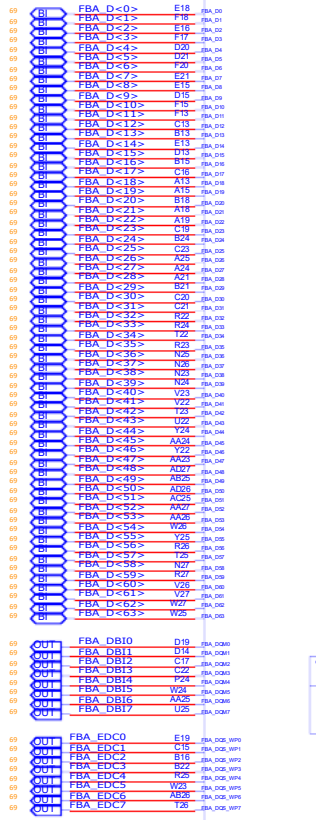


Figure 7-3. Reset Signal Connection

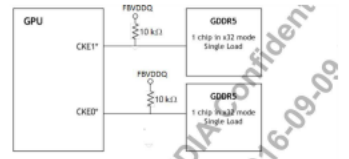


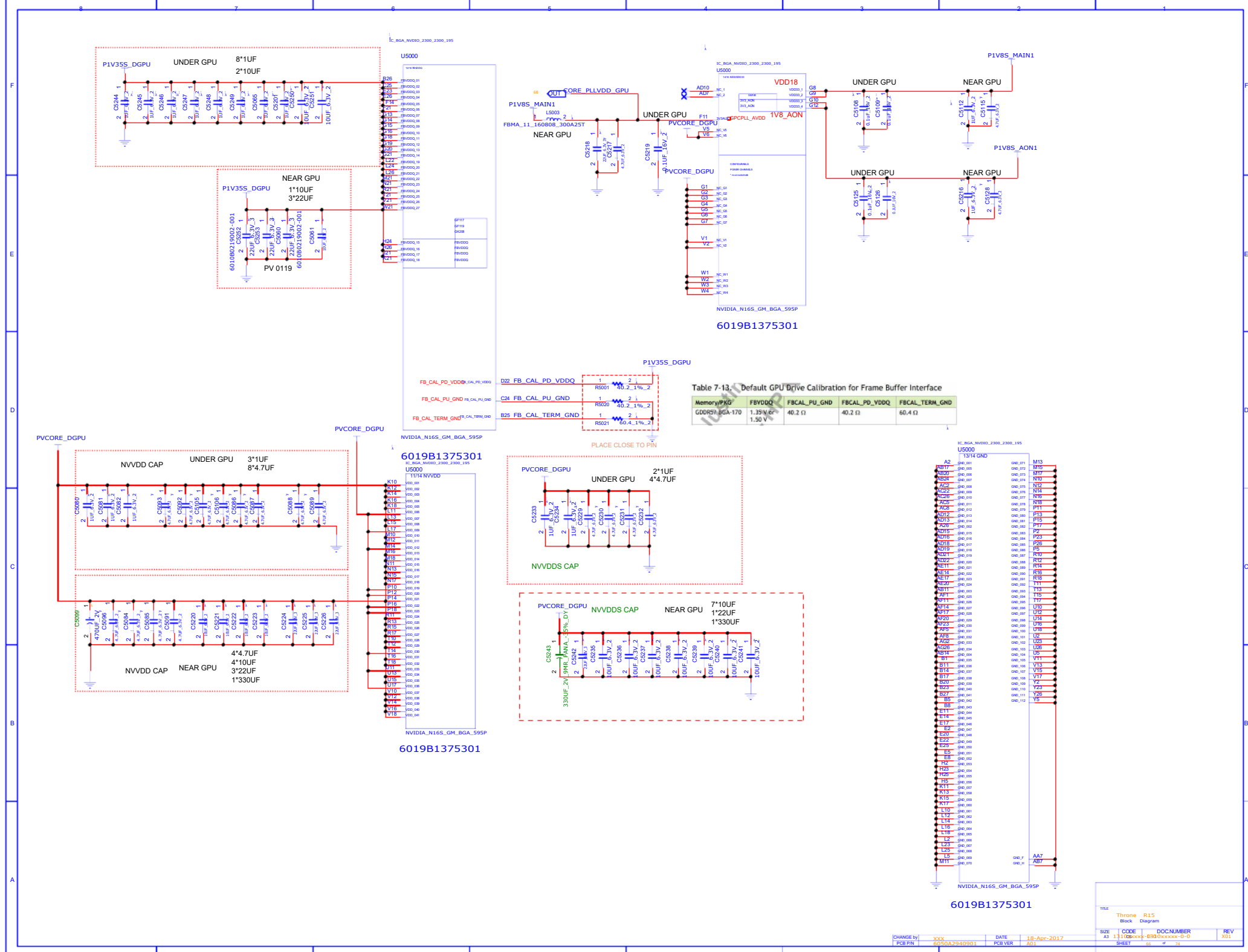
Figure 7-4. Clock Enable (CKE) Signal Connection, x32 Mode

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABJ*	CMD24	ABJ*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128 Channel 0 & 1			
CMD32	Not used		
CMD33 ¹	Not used		
CMD34	DEBUG0 ²		
CMD35	DEBUG1 ²		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.

6019B1375301

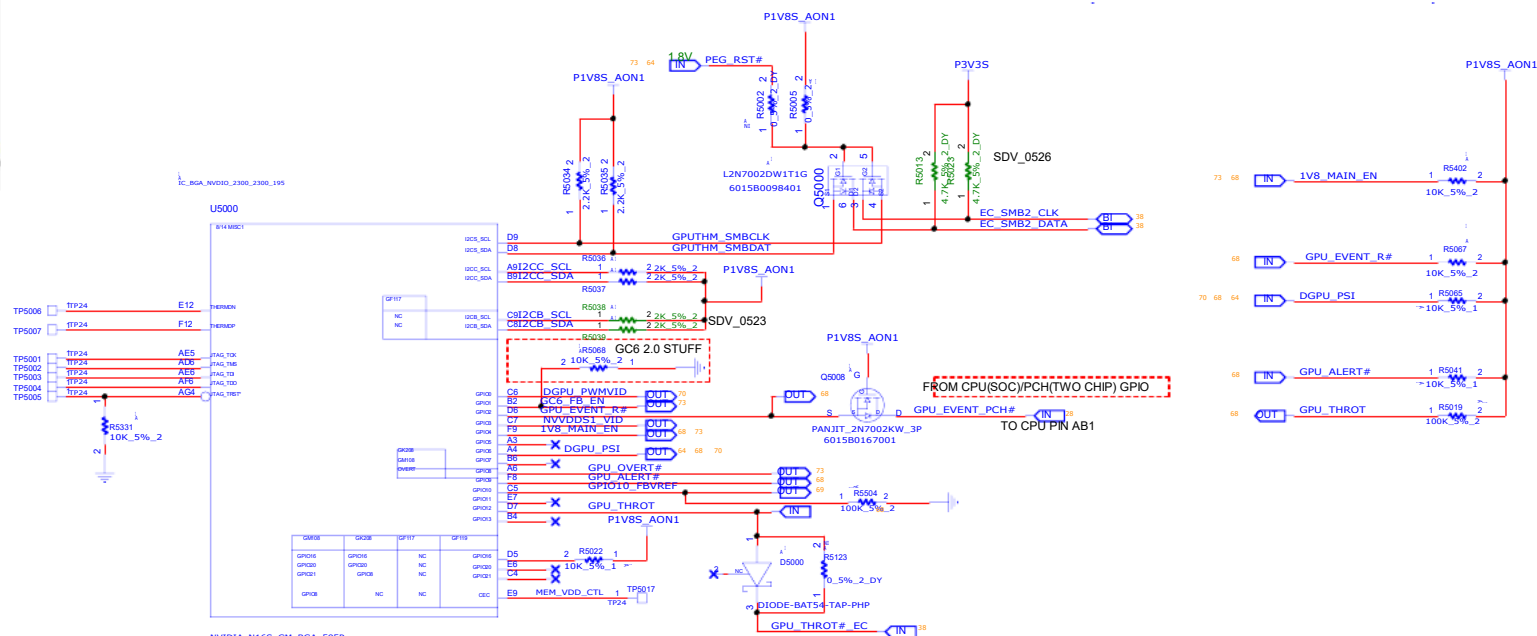
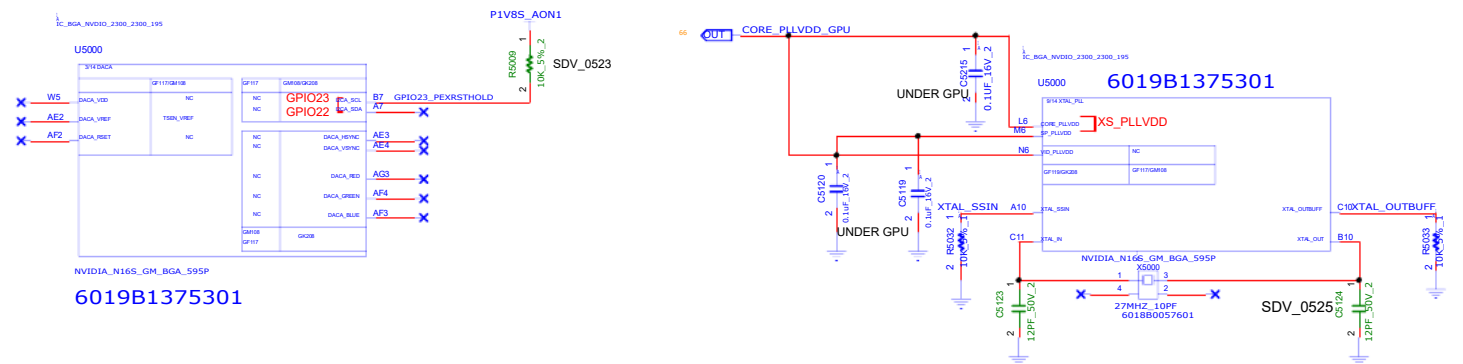




Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCL	N155-GH-07 N155-GH-07 All Q82-A4 N14 and Q84-A15	PCL_DEV0[3] SMB_DEV0[3]	SMB_VENDOR SMB_DEV0[2]	PCL_DEV0[1] SMB_DEV0[1]	PCL_PLL_CLK_TEN0 SMB_DEV0[0]
ROM_S1	N155-GH-07 N14 and Q84-A15	RAM_CFG[3] RAN_CFG[3]	RAN_CFG[2] RAN_CFG[2]	RAM_CFG[1] RAN_CFG[1]	
ROM_S0	N155-GH-07 N155-GH-07	FR[1] DEVID_SEL		SMB_ADDR_ADD0	VGA_DEVICE
STRAP0	N155-GH-07 N155-GH-07	USER[3] DEVID_SEL	P_CIE_CFG	USER[1]	USER[0]
STRAP1	N155-GH-07 N155-GH-07	Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default) SMB_PADCFG[3] SMB_PADCFG[3]	SMB_PADCFG[2] SMB_PADCFG[2]	SMB_PADCFG[1] SMB_PADCFG[1]	SMB_PADCFG[0] SMB_PADCFG[0]
STRAP2	N155-GH-07 N155-GH-07	Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default) PCL_DEV0[3] PCL_DEV0[3]	PCL_DEV0[2] PCL_DEV0[2]	PCL_DEV0[1] PCL_DEV0[1]	PCL_DEV0[0] PCL_DEV0[0]
STRAP3	N155-GH-07 N155-GH-07	SMB_EXPOSED SMB_EXPOSED	SMB_EXPOSED SMB_EXPOSED	SMB_EXPOSED SMB_EXPOSED	SMB_EXPOSED SMB_EXPOSED
STRAP4	N155-GH-07 N155-GH-07	Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default) Reserved Reserved	P_CIE_SPEED_CFG NGL_DEV0[3]	P_CIE_AXP_SPEED P_CIE_AXP_SPEED	PLL_VDD037 PLL_VDD037
	N155-GH-07 N155-GH-07	Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default) Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)			

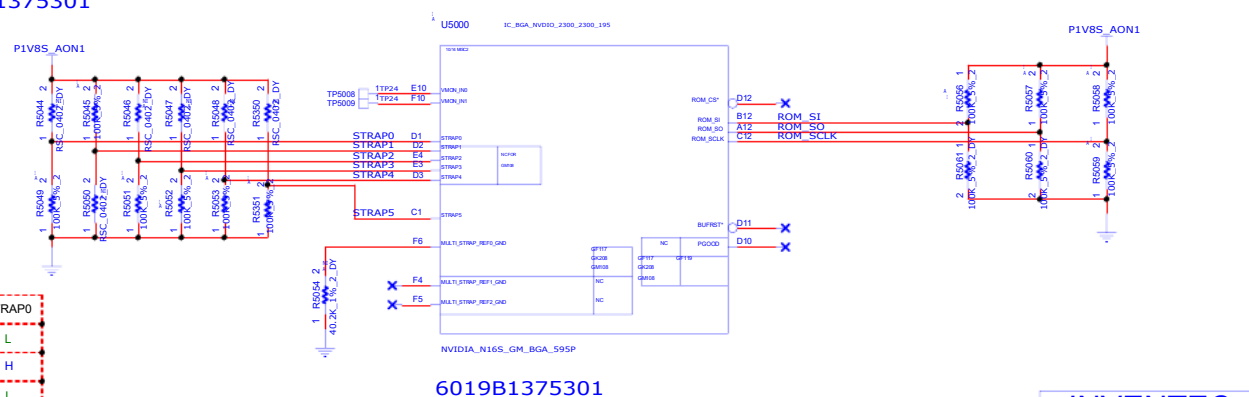
This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVICE straps. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific Platform Update Notification for the latest configuration.

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3GIO_PADCFG. This strap only exists in the GB26-64 and GB2B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific Platform Update Notification for the latest configuration.



Strap Pins <small>see Note</small>			RANCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (rx0000)
L	L	H	1 (rx0001)
L	H	L	2 (rx0002)
L	H	H	3 (rx0003)
H	L	L	4 (rx0004)
H	L	H	5 (rx0005)
H	H	L	6 (rx0006)
H	H	H	7 (rx0007)
L	L	M	8 (rx0008)
L	M	L	9 (rx0009)
L	M	M	10 (rx000A)
L	M	H	11 (rx000B)
M	L	L	12 (rx000C)
M	L	H	13 (rx000D)

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	STRAP2	STRAP1	STRAP0
SAMSUNG	256MX32	K4G80325FB-HC28	6019B1485901	0X0	L	L	L
MICRON	256MX32	MT51J256M32HF-70.A	6019B1486001	0X1	L	L	H
HYNIX	256MX32	H5GC8H24MJR-ROC	6019B1542101	0X2	L	H	L



INVENTEC

TITLE			
Throne R15			
GPU-5			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxxx-0-0	X01
SHEET		68	of 74

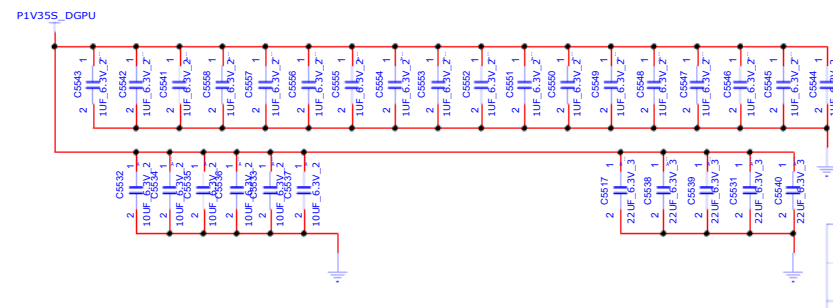
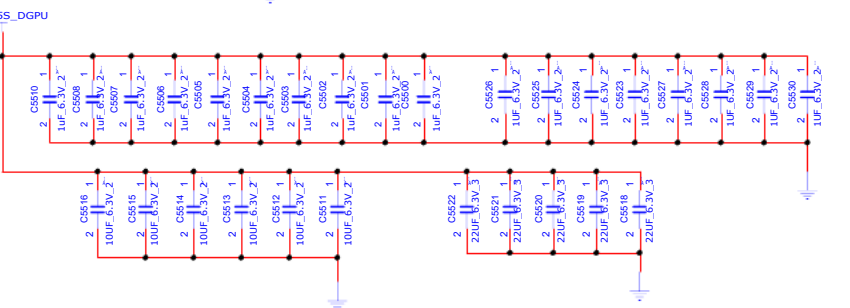
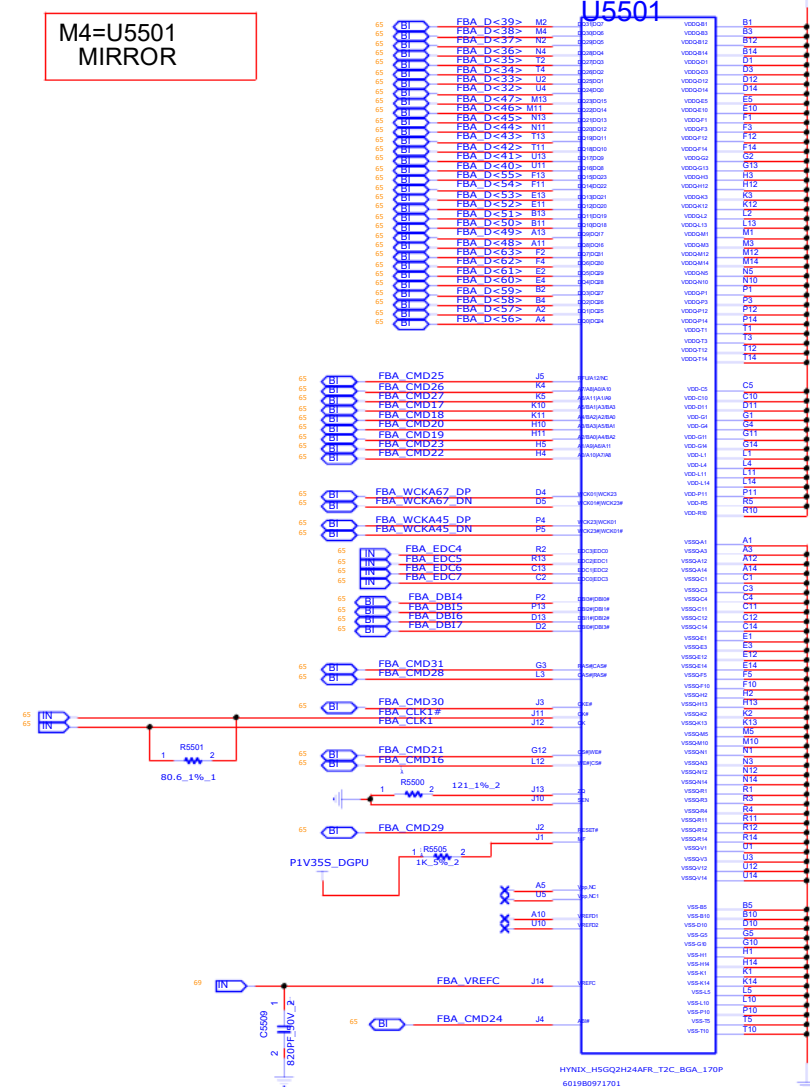
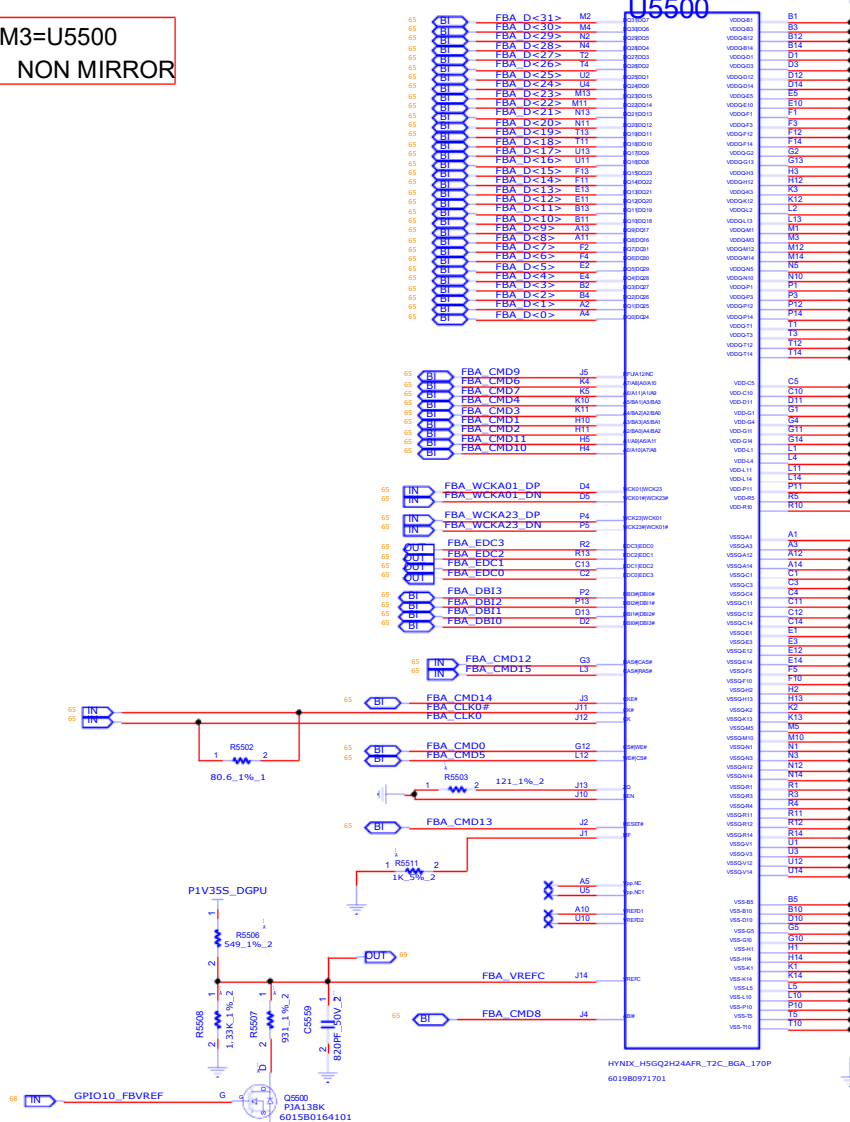
MEMORY: FBA Partition 31.0
MEMORY: FBA Partition 63.32

M3=U5500
NON MIRROR

P1V35S_DGPU

M4=U5501
MIRROR

P1V35S_DGPU

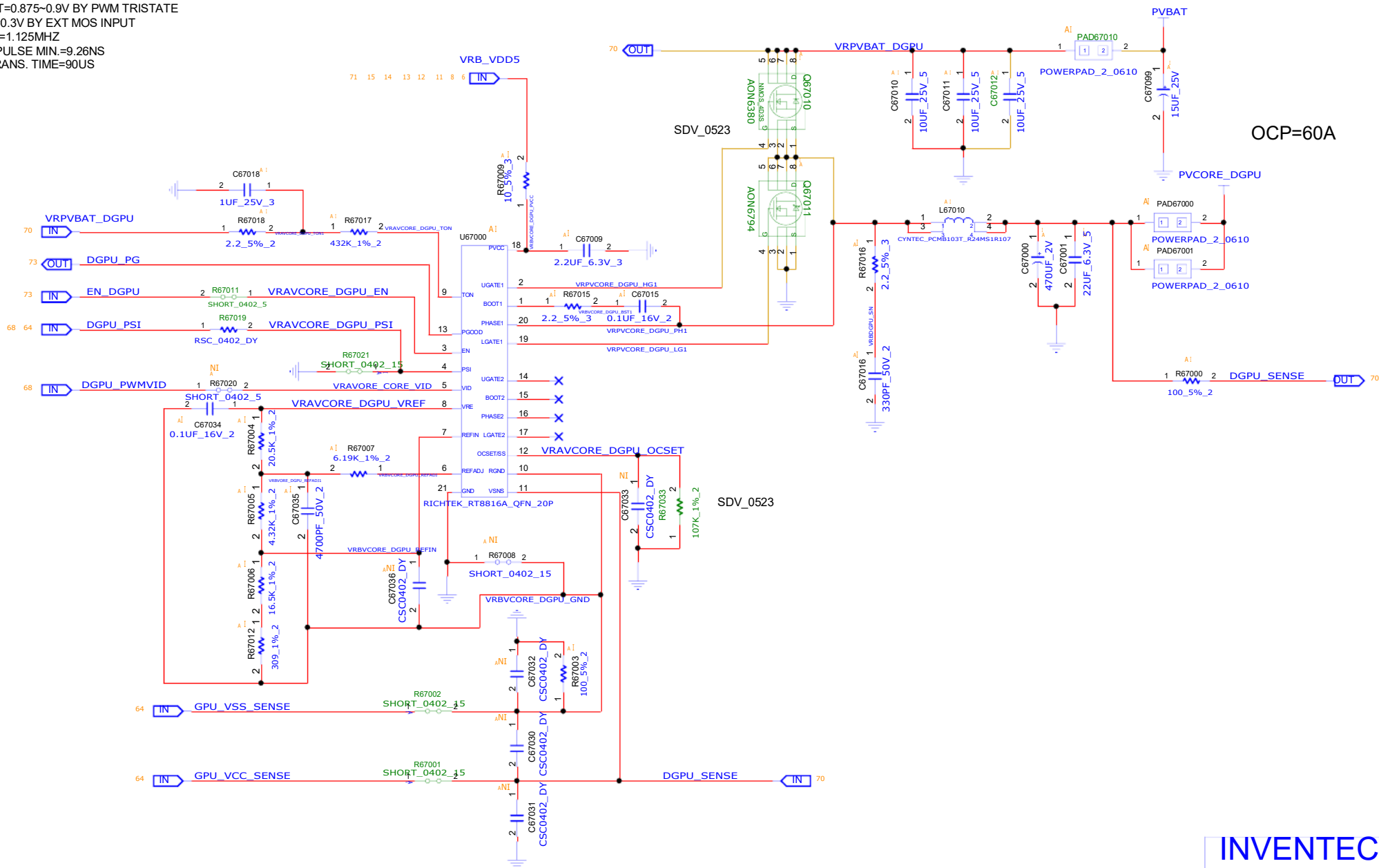


INVENTEC

Throne R15
Block Diagram
SIZE CODE QCCNUMBER REV
C CS 1310xxxxx-0-0 X01
SHEET 69 24

CHANGE BY XXX GUSSENKOS01 DATE 18.AUG.2017
PCB PN PCB VER

VMAX=1.2V BY PWM D=100%
 VMIN=0.6V PWM D=0%
 VBOOT=0.875-0.9V BY PWM TRISTATE
 VSTB=0.3V BY EXT MOS INPUT
 FPWM=1.125MHZ
 PWM PULSE MIN.=9.26NS
 VID TRANS. TIME=90US

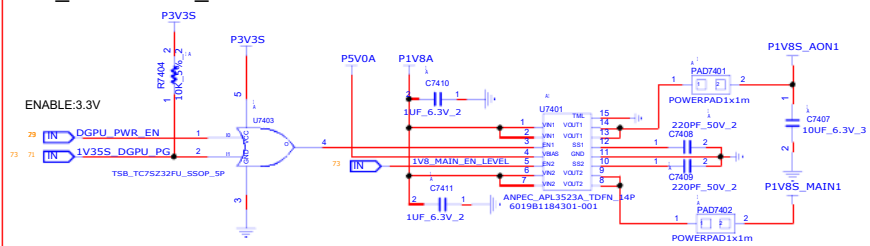


INVENTEC

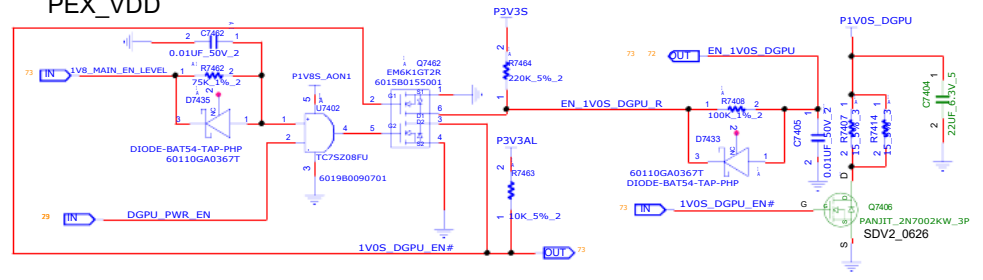
CHANGE by	XXX	DATE	18-Apr-2017	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	6050A2940901	PCB VER	A01	SHEET	70	of	74		

POWER_ON: P1V8S_AON1-->P1V8S_MAIN1-->NVVDD-->PEX_VDD-->FBVDD
POWER_OFF: FBVDD-->PEX_VDD-->NVVDD-->P1V8S_MAIN1-->P1V8S_AON1

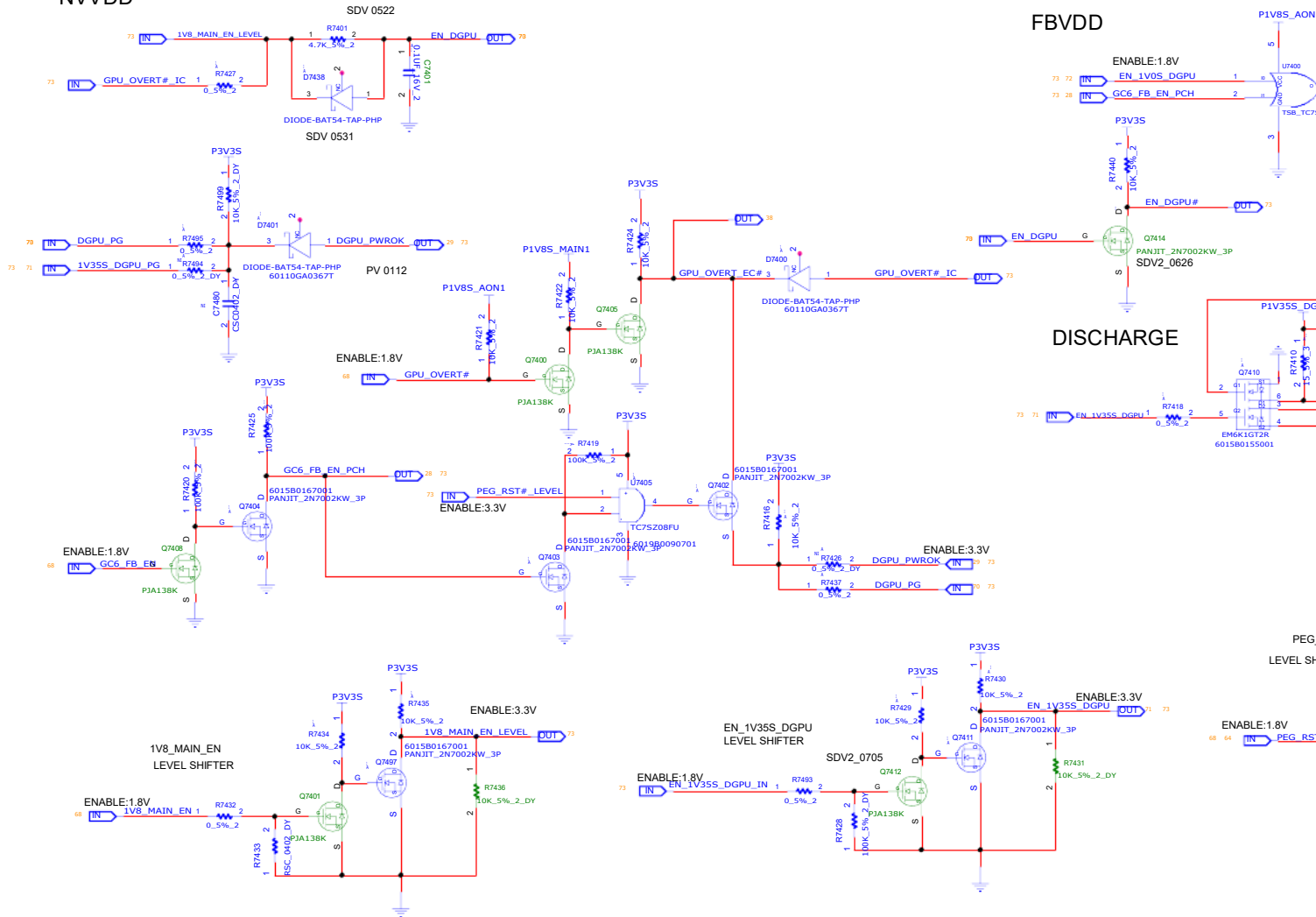
1V8_AON & 1V8_MAIN



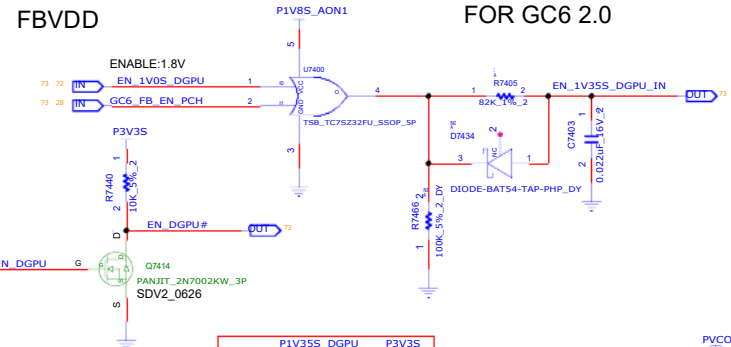
PEX_VDD



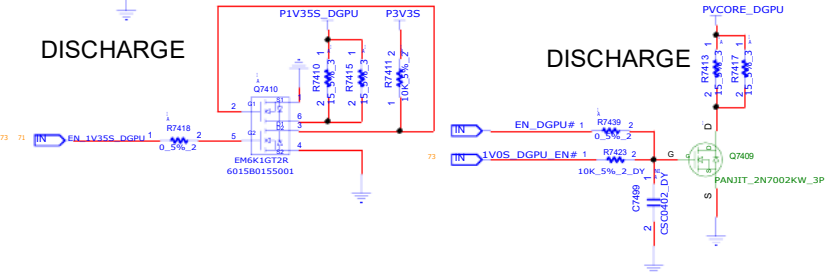
NVVDD



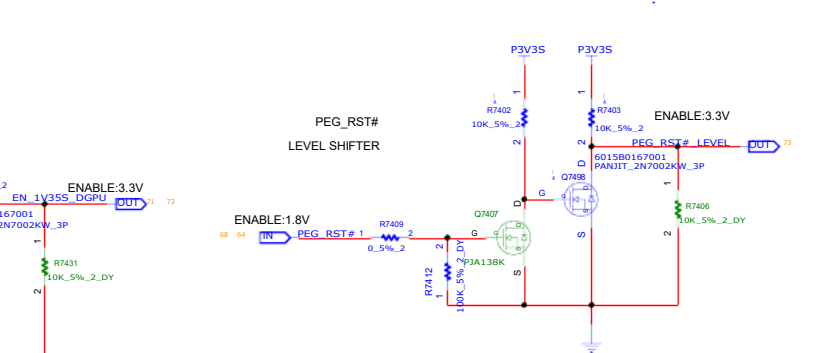
FBVDD



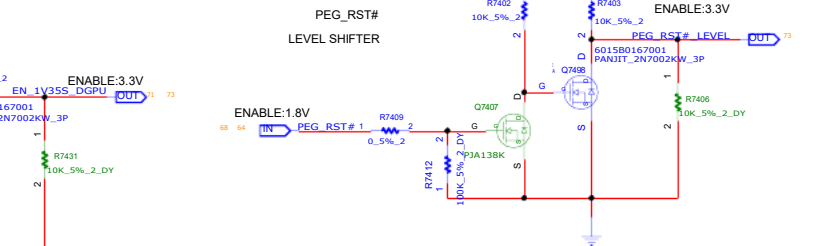
FOR GC6 2.0



DISCHARGE



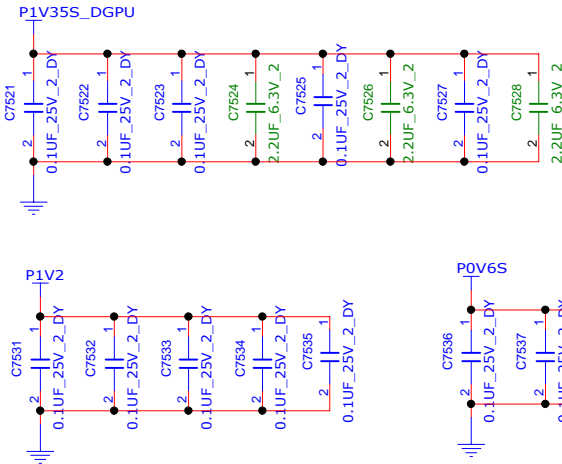
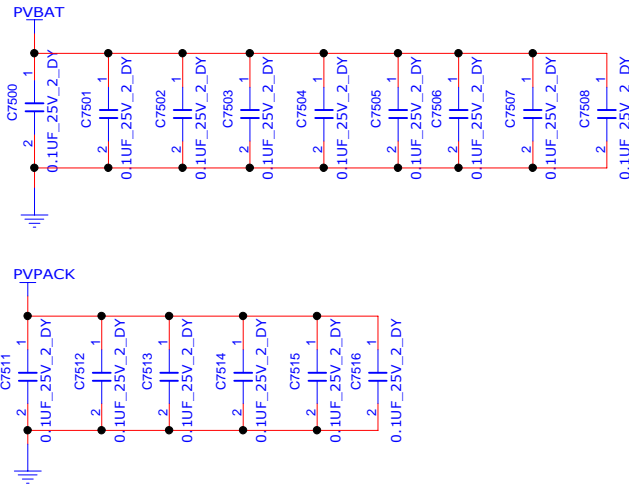
PEG_RST#
LEVEL SHIFTER



INVENTEC

TITLE			
Throne R15 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 73 of 74			

RF&EMI



INVENTEC

TITLE			
Throne R15 Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		74 of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01